Prince of Songkla University

Facultry of Engineering

Department of Computer Engineering

Final Exam session 1 Year 2002

Date 26 September 2002 Time 9.00-12.00

Subject 240-233 Principles of Digital Systems Room R200, R201

- There are 7 questions. Answer all questions.
- All questions are of difference values.
- Calculator, textbooks and hand-out are prohibited
- Every questions must be clear and show how to get the answer.

NOTE

- All answers must be given in ink.
- Unless otherwise indicated, pencils should only be used for graphical work.

Name :_____Student ID:_____

Question	1	2	3	4	5	6	7	Total
Scores								

1. Determine the state of each flip-flop waveform of Figure 1 (a) after each clock pulse. Data and the clock and SHIFT / $\overline{\text{LOAD}}$ waveform are given in Figure 1 (b). Assume that the flip-flops are initially RESET.

(10 points)

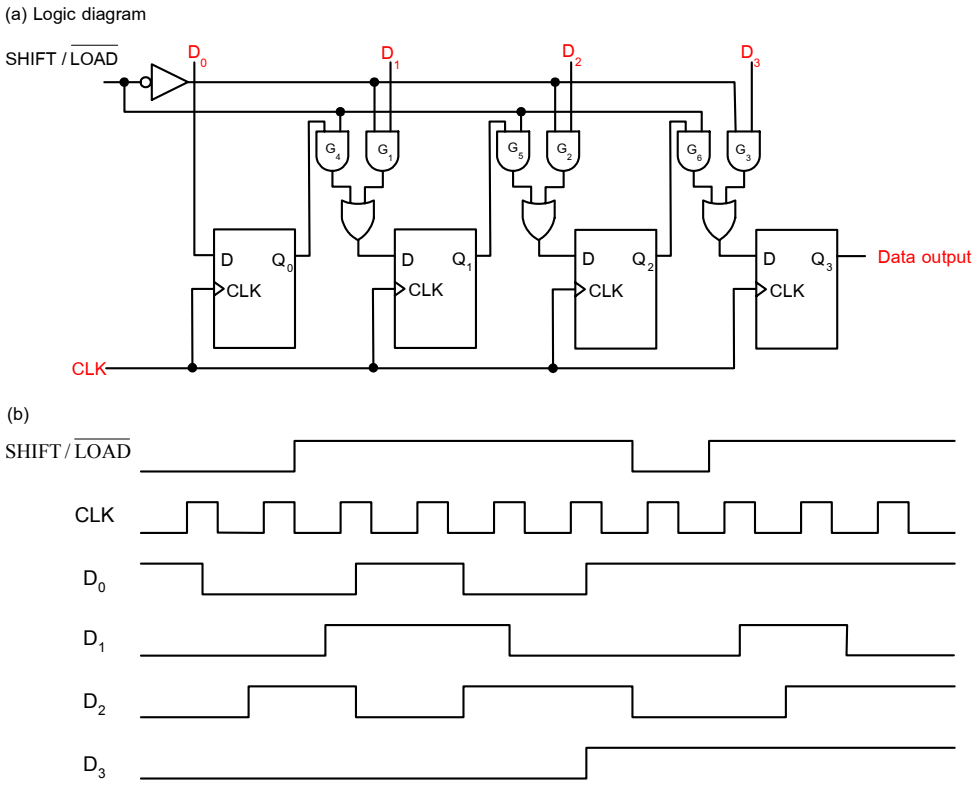


Figure 1

Answer : Q_0 _____

Q_1 _____

Q_2 _____

Q_3 _____

2. Design Full adder circuits by using NAND gate only. (15 points)

Answer

3. Consider the circuit of Figure 2. Initially all FFs are in the 0 state. The circuit operation begins with a momentary start pulse applied to the $\overline{PRESET}$ inputs of FFs X and Y. Determine the waveforms at A, B, C, X, Y, Z, and W for 20 cycles of the clock pulses after the start pulse. State all assumptions. (20 points)

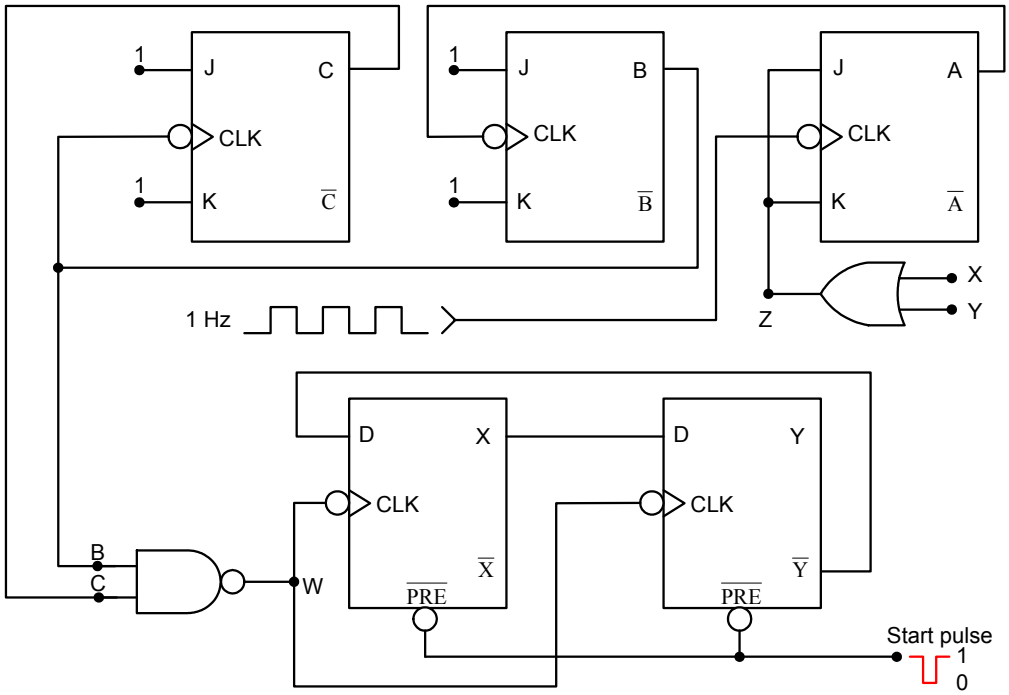
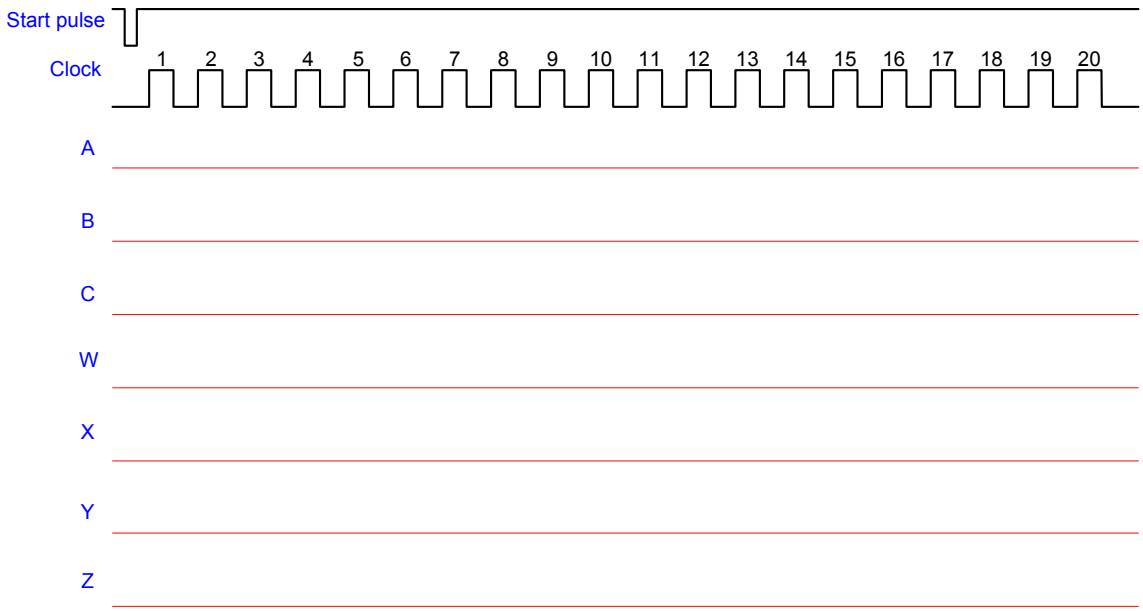


Figure 2



4. (a) Show how a 74LS74s counter can be used to produce a 1.2-kpps output from an 16.8 kpps input. (See Appendix) (5 points)

(b) Determine the frequency at output X in figure 3.(See Appendix) (5 points)

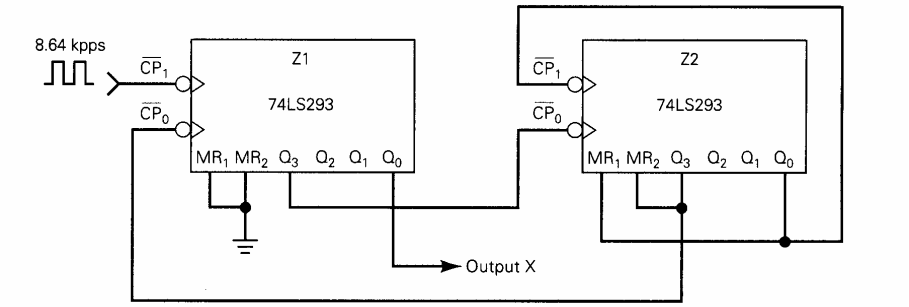


Figure 3

5. Figure 4 shows the basic circuitry to interface a microprocessor (MPU) to a memory module. The memory module will contain one or more memory ICs that can either receive data from the MPU (a WRITE operation) or send data to the MPU(a READ operation). The data are transferred over the eight-line data bus. The MPU's data lines and the memory's I/O data lines are connected to this common bus. For now we will be concerned with how the MPU controls the selection of the memory module for a READ or WRITE operation.

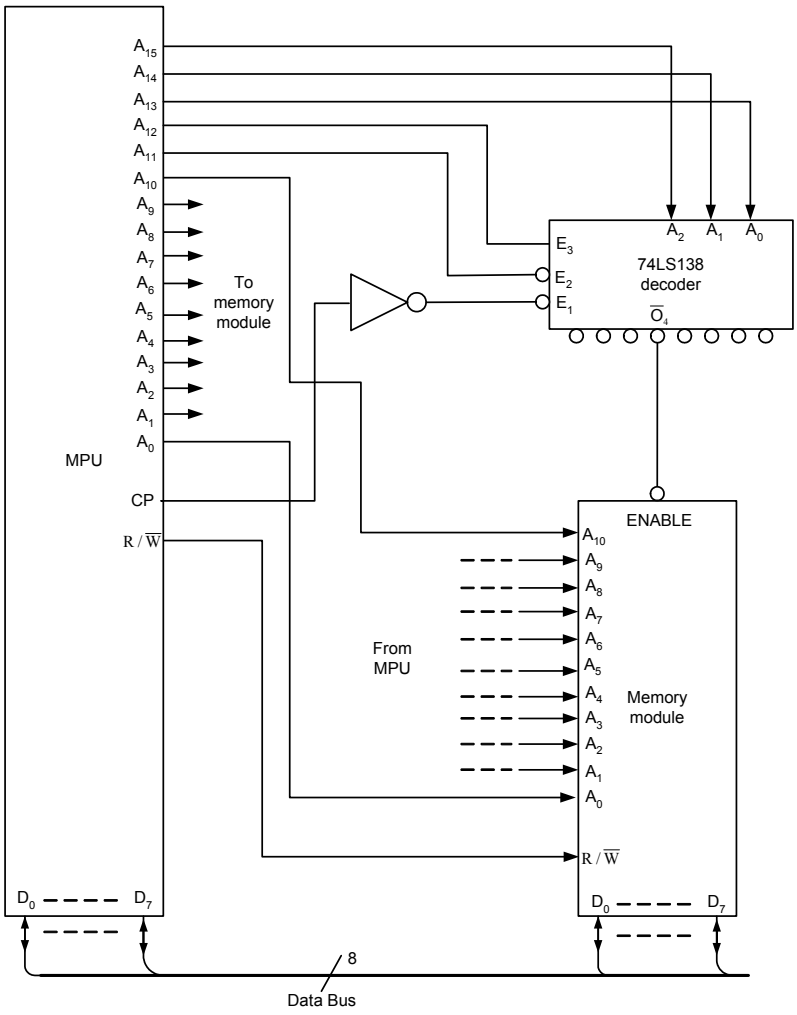


Figure 4

The steps involved are as follows:

1) The MPU places the memory address on its address output lines A_{15} to A_0.
2) The MPU generates the $R/\overline{W}$ signal to inform the memory module which operation is to be performed: $R/\overline{W} = 1$ for READ, $R/\overline{W} = 0$ for WRITE.

3) The upper five bits of the MPU address lines are decoded by the 74LS138, which controls the ENABLE input of the memory module. This ENABLE input must be active in order for the memory module to do a READ or WRITE operation.
4) The other 11 address bits are connected to the memory module, which uses them to select the specific internal memory location being accessed by the MPU, provided that ENABLE is active.

In order to read from or write into the memory module, the MPU must put the correct address on the address lines to enable the memory, and then pulse CP to the HIGH state.

(a) Determine what range of hex addresses will activate the memory.(Hint: Inputs A_0 to A_{10} to memory can be any combination.) (5 points)

(b) Assume that a second identical memory module is added to the circuit the first module except that its ENABLE input is tied to decoder output $\overline{O}_2$. What range of hex addresses will activate this second module? (5 points)

6. Design a synchronous counter that has the following sequence: 000, 010, 101, 110, and repeat. The undesired(unused) state 001, 011, 100 and 111 must always go to 000 on the NEXT clock pulse. Use D-Flip-Flop. (20 points)

7. What are the differences between LATCH and FLIP-FLOP, OS and Timer 555?

(5 points)

Appendix

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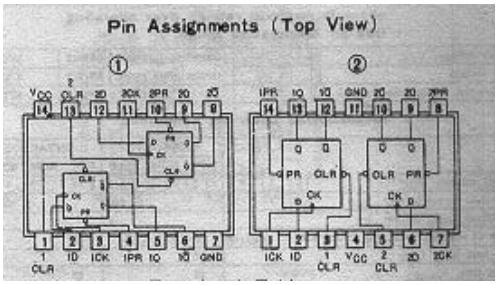


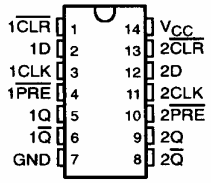
(a)

SN54AHC74, SN74AHC74
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

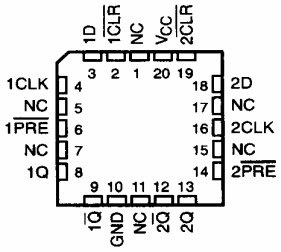
SCLS255E – DECEMBER 1995 – REVISED NOVEMBER 1998

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

SN54AHC74 . . . J OR W PACKAGE
SN74AHC74 . . . D, DB, DGV, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHC74 devices are dual positive-edge-triggered D-type flip-flops.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54AHC74 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC74 is characterized for operation from –40°C to 85°C.

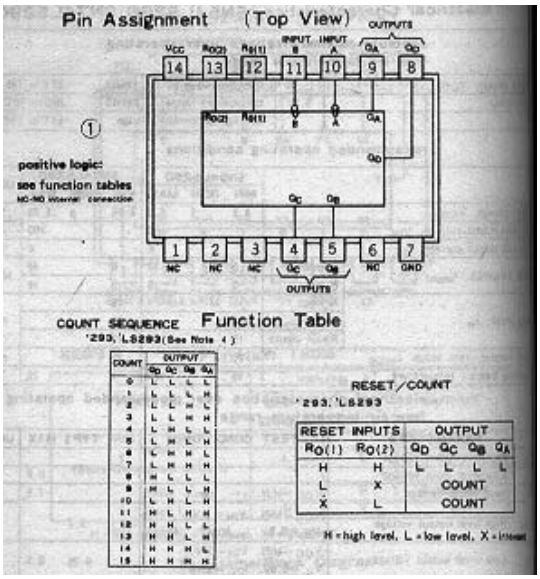
FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

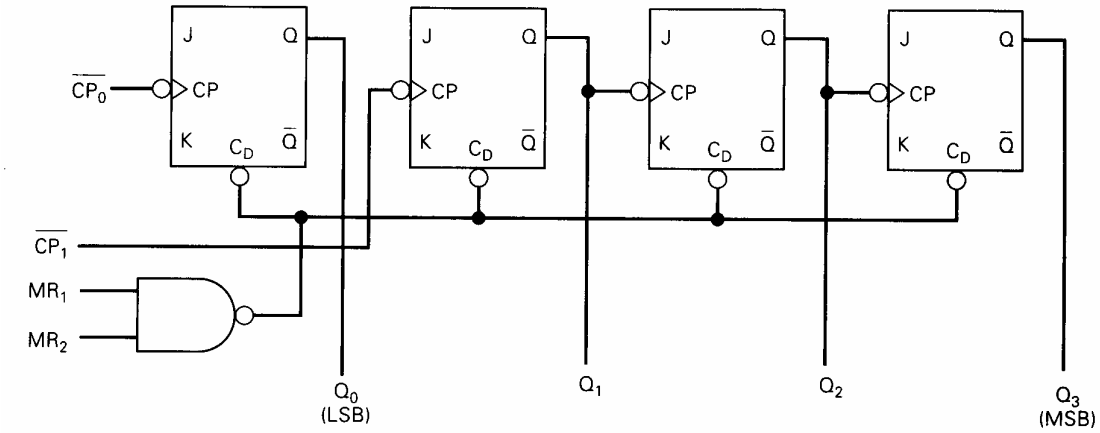
† This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

(b)

74LS293

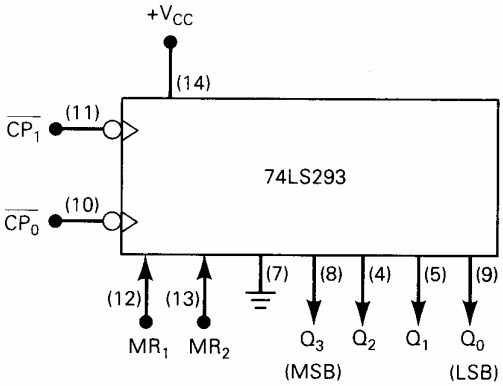


74LS293



*All J, K inputs are internally connected HIGH.

(a)



(b)