## PRINCE OF SONGKLA UNIVERSITY <br> FACULTYOF ENGINEERING

| Examination : Final - Session 1 | Year : 2003 |
| :--- | :--- |
| Date : 2 October 2003 | Time : 9.00-12.00 |
| Subject : 240-205 Digital Systems and Logic Design | Room : |

## NOTE

- There are 7 questions 13 pages. Answer all questions
- All questions are of different values.
- Calculator, textbooks and hand-out are prohibited.
- Every answer must be clear and show how to get the answer.
- All answers must be given in ink.
- Unless otherwise indicated, pencils should only be used for graphical work.

Student ID : $\qquad$ Name : $\qquad$ Section : $\qquad$

| Question | Points |  |
| :---: | :---: | :--- |
| 1 | 8 |  |
| 2 | 5 |  |
| 3 | 12 |  |
| 4 | 10 |  |
| 5 | 10 |  |
| 6 | 5 |  |
| 7 | 20 |  |
| Total | $\mathbf{7 0}$ |  |

Student ID :
Name:

1. Determine the state of each flip-flop waveform of figure 1 (a) after each clock pulse. The Data, clock and SHIFT/LOAD waveforms are given in figure 1 (b). Assume that the flip-flops are initially RESET.
(8 points)
(a) Logic diagram

(b)


Figure 1

## Answer

$Q_{0}$
$Q_{1}$
$Q_{2}$
$Q_{3}$

Student ID :
2. Determine the frequency at output X and $\mathrm{Q}_{\mathrm{D}}$ in figure 2 when input clock is 8.64 kpps .
(5 points)


Figure 2
Answer
$\longrightarrow$
-
$\qquad$
$\qquad$
$\qquad$
$\qquad$
$\qquad$

Student ID :
Name:
3. Figure 3 shows how a decoder can be used in the generation of control signals. Assume that a RESET pulse has occurred at time $t_{0}$, determine the $A_{3}, A_{2}, A_{1}, E_{3}, \bar{E}_{2}$ and CONTROL waveforms for 24 clock pulses. (12 points)


RESET

$\qquad$
$\qquad$
$\qquad$
$\qquad$
$\qquad$
$\qquad$
$\qquad$

## Student ID :

Name:
4
4. Show how two 74LS293s can be connected to divide an input frequency by 20 while producing a symmetrical square-wave output. (10 points)

## Answer

Student ID : Name:
5. Design the Full Adder by using NAND gates. (10 points) Answer

Student ID : Name:
6. Design 16-input multiplexer by using 74LS151.(Give more detail how to design)
(5 points)

## Answer

Student ID :
Name:
7. (a) Design a synchronous MOD-6 UP/ $\overline{D O W N}$ counter by using MC14013B (See appendix). The counter should count up when an $U P / \overline{D O W N}$ control input is 1 and count down when the control input is 0.
(10 points)
Answer

Student ID :
Name:

Student ID :
Name:
(b) Draw a logic diagram of the problem 7 (a) (10 points)




## Appendix


(a)

| Inputs |  |  |  | Outputs |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\overline{\mathrm{E}}$ | $\mathrm{S}_{2}$ | $\mathrm{S}_{1}$ | $\mathrm{S}_{0}$ | $\bar{Z}$ | Z |
| H | X | X | X | H | L |
| L | L | L | L | $\bar{I}_{0}$ | $\mathrm{I}_{0}$ |
| L | L | L | H | $\underline{I}_{1}$ | $\mathrm{I}_{1}$ |
| L | L | H | L | $\mathrm{I}_{2}$ | $\mathrm{I}_{2}$ |
| L | L | H | H | $\mathrm{I}_{3}$ | $\mathrm{I}_{3}$ |
| L | H | L | L | $\mathrm{I}_{4}$ | $\mathrm{I}_{4}$ |
| L | H | L | H | $\mathrm{I}_{5}$ | $I_{5}$ |
| L | H | H | L | $\underline{I}_{6}$ | $\mathrm{I}_{6}$ |
| L | H | H | H | $\mathrm{T}_{7}$ | $\mathrm{I}_{7}$ |


(c)
(b)

## 74LS151

74LS293


## MC14013B Dual Type D Flip-FLop

Block Diagram


Truth Table

| Inputs |  |  |  | Outputs |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| clock $^{\dagger}$ | data | reset | set | Q | $\overline{\mathrm{Q}}$ |
|  | 0 | 0 | 0 | 0 | 1 |
|  | 1 | 0 | 0 | 1 | 0 |
|  | X | 0 | 0 | Q | $\overline{\mathrm{Q}}$ |
|  | no change |  |  |  |  |
| X | X | 1 | 0 | 0 | 1 |
| X | X | $\mathbf{0}$ | 1 | 1 | $\mathbf{0}$ |
| X | X | 1 | 1 | 1 | 1 |

X = Don't Care
$\dagger$ = Level Change

Student ID :
Name:
74138


