PRINCE OF SONGKLA UNIVERSITY FACULTY OF ENGINEERING

Examination: Final - Session 1 Year: 2003

Date: 2 October 2003 Time: 9.00-12.00

Subject: 240-205 Digital Systems and Logic Design Room:

NOTE

- There are 7 questions 13 pages. Answer all questions
- All questions are of different values.
- Calculator, textbooks and hand-out are prohibited.
- Every answer must be clear and show how to get the answer.
- All answers must be given in ink.
- Unless otherwise indicated, pencils should only be used for graphical work.

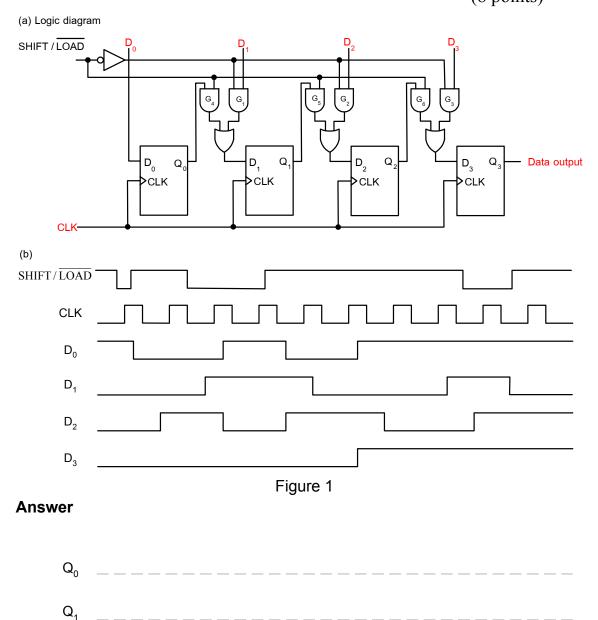
Student ID:	Name:	Section:
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Question	Points	
1	8	
2	5	
3	12	
4	10	
5	10	
6	5	
7	20	
Total	70	

Student ID: Name:

1. Determine the state of each flip-flop waveform of figure 1 (a) after each clock pulse. The Data, clock and SHIFT/LOAD waveforms are given in figure 1 (b). Assume that the flip-flops are initially RESET.

(8 points)



 Q_2

 Q_3

Student ID :	N T	<u> </u>
Student III.	Name:	,
Jiuuchi ID.	ranic.	_

2. Determine the frequency at output X and Q_D in figure 2 when input clock is 8.64 kpps. (5 points)

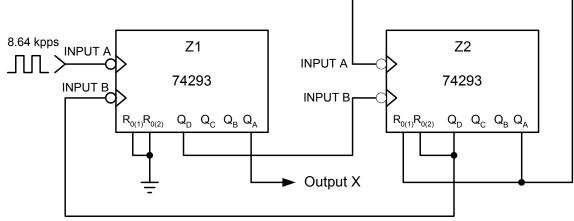
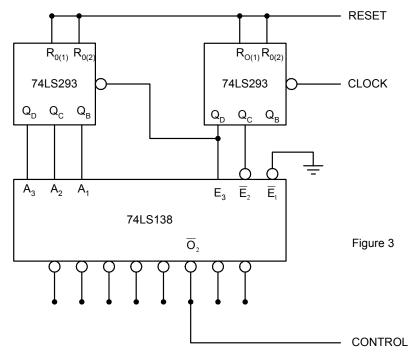


Figure 2

Answer				

Student ID: Name:	3
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3. Figure 3 shows how a decoder can be used in the generation of control signals. Assume that a RESET pulse has occurred at time t_0 , determine the A_3 , A_2 , A_1 , E_3 , \overline{E}_2 and CONTROL waveforms for 24 clock pulses. (12 points)



RESE	T_																																
CLK					Л		Ш		П		Ш		П		Ш	L					l			Ш		Л		Ш			Л		L
	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_		_
	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_		_
	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
	_	_					_											_								_	_	_	_	_	_	_	

ANSWER

Stı	ıdent ID :	Name: 4
	Show how	w two 74LS293s can be connected to divide an input by 20 while producing a symmetrical square-wave output. (10 points)
Ar	iswer	

Student ID:	Name:		5
5. Design the I Answer	Full Adder by using NAND	gates.	(10 points)

Design 16-input multiplexer by using 74LS151.(Give more detail how to design) (5 points)	
nswer(5 points)	
HSWC1	_
	_
	_
	_
	_
	_
	_
	_
	_
	_
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	_
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Student ID :	N	lame:			7
MC14013B	a synchronous (See appendix). control input is 1	The co	unter should	count up	when an
0.	1				points)
Answer					

Student ID:	Name:	8

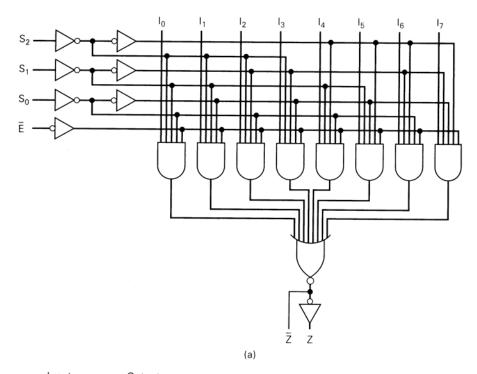
Student ID: Name:
(b) Draw a logic diagram of the problem 7 (a)

D Q MC14013B

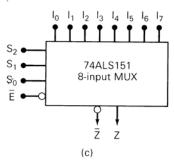
MC14013B C <u>Q</u> \simeq

MC14013B

Appendix

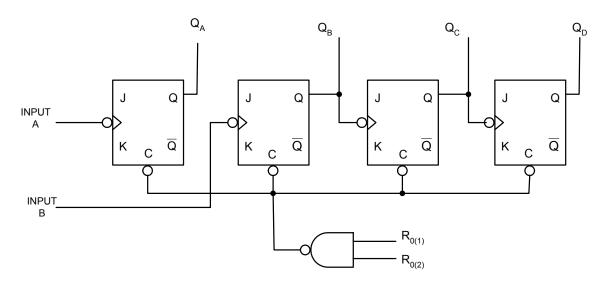


Inputs					Outputs		
Ē	S ₂	S ₁	S ₀		ž	Z	
H	X	X L L H H L L H H	X		H ₁₀ -1-2-3-4-5-6-7	L I ₀ I ₁ I ₂ I ₃ I ₄ I ₅ I ₆ I ₇	
(b)							

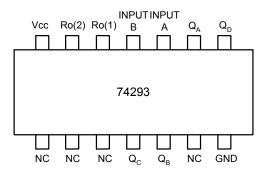


74LS151

74LS293

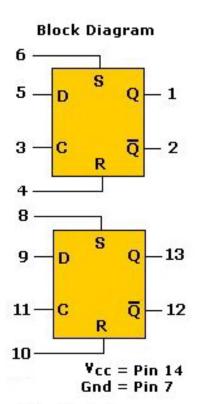


RESET	INPUTS	OUTPUT			
R0(1)	R0(2)	Q_D	Q_{C}	Q_{B}	Q_A
Н	Н	L	L	L	L
L	Х	L	L	L	Н
Χ	L	L	L	Н	L



	OUTPUT					
Count	Q_D	Q_{C}	Q_B	Q _A		
0	L	L	L	L		
1	L	L	L	Н		
1 2 3 4 5	L L	L	Н	L		
3	L	L	Н	Н		
4	L	Н	L	L		
	L	Н	L	Н		
6	L	Н	Н	L		
7	L	Н	Н	Н		
8	Н	L	L	L		
9	Н	L	L	Н		
10	Н	L	Н	L		
11	Н	L	Н	Н		
12	Н	Н	L	L		
13	Н	Н	L	Н		
14	Н	Н	Н	L		
15	Н	Н	Н	Н		

MC14013B Dual Type D Flip-FLop



Truth Table

The state of the s								
Inputs				Outputs				
clock [†]	data	reset	set	Q	Q	3		
	0	0	0	0	1			
	1	0	0	1	0			
	х	0	0	Q	Q	no c		
Х	Х	1	0	0	1	8		
Х	Х	0	1	1	0	8		
Х	х	1	1	1	1	8		
(757)	3333	3/4/2	2,0	55.00	5,835			

no change

X = Don't Care † = Level Change Student ID: Name: 13

74138

