PRINCE OF SONGKLA UNIVERSITY

FACULTY OF ENGINEERING

Examination : Mid Exam - Session 2 Year : 2003
Date : 27 Dec 2003 Time :13.30-16.30
Subject : 240-205 Digital Systems and Logic Design Room :

NOTE

- There are 7 questions 14 pages (not include cover page). Answer all questions
- All questions are of different values.
- Calculator, textbooks and hand-out are prohibited.
- Every answer must be clear and show your working to get the answer.
- All answers must be given in ink, in English
- Unless otherwise indicated, pencils should only be used for graphical work.

Student ID :_____Name :_____Section : _____

Question	1	2	3	4	5	6	7
Scores							

Q1. A repetitive pulse waveform has a logic 1 for 1 ms and a logic 0 for 7 ms in each period.

(a) What is the period of the waveform? (2 marks)

Answer

(b) What is the frequency of the waveform? (2 marks)

Answer

(c) What is the duty cycle of the waveform ? (3 marks)

Answer

(d) What is the average rise time, t_{LH} and fall time t_{HL} if the gate used to generate this waveform is a type 74LS08? (See appendix for data sheets) (3 marks)

Answer

Q2. (a) What is the binary equivalent of 10.375 ? (3 marks)

Answer

(b) What is the number range of an 8 bit 2's complement number? (3 marks)

Answer

(c) Express -42 as a 2's complement number (3 marks)

Answer

(d) Express -0.1 as a 9 bit 2's complement number. (3 marks)

Answer

(e) Divide the 2's complement number 10000011 by 00011001

(4 marks)

Answer

(f) Add the BCD number 01100111 with 01011001

(4 marks)

Answer

Q3.

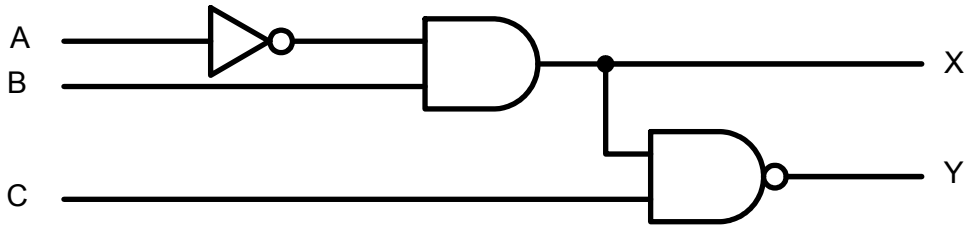


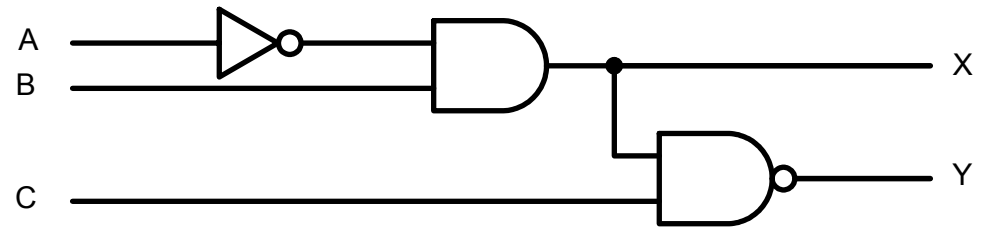
Fig 1

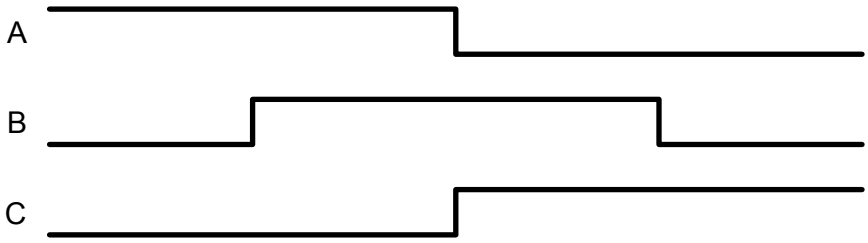
(a) Identify the logic function X and Y (2 marks)

Answer

(b) Sketch the waveforms X and Y, taking into account the gate propagation delays (assume all gates have a propagation delay of 8 ns) (4 marks)

Answer





(c) What is the longest period when the Y output is incorrect ?

(4 marks)

Answer

Q4.

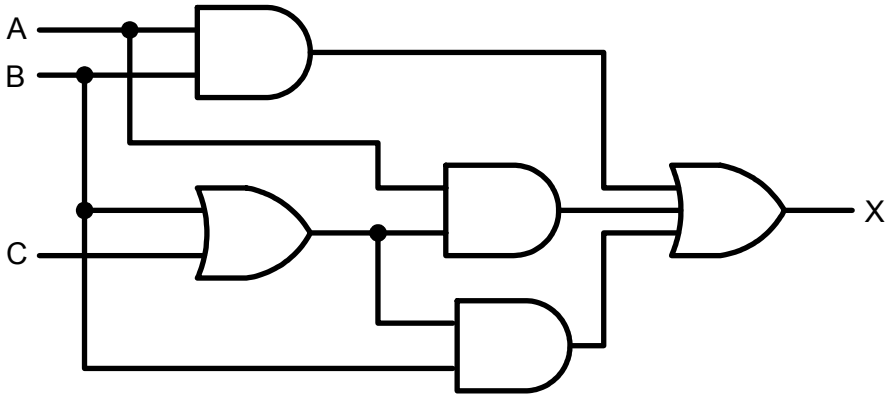


Fig.2

(a) Simplify the circuit of Fig.2 using Boolean algebra.

(3 marks)

Answer

(b) Draw the simplified logic circuit and construct the truth table

(2 marks)

Answer

Q5. (a) Draw the Karnaugh map for the standard SOP expression

$$X = \overline{D}\overline{C}\overline{B}\overline{A} + \overline{D}\overline{C}B\overline{A} + \overline{D}\overline{C}BA + \overline{D}C\overline{B}\overline{A} + \overline{D}C\overline{B}A + \overline{D}CBA + D\overline{C}\overline{B}\overline{A} + D\overline{C}\overline{B}A + D\overline{C}B\overline{A} + DC\overline{B}A + DCB\overline{A}$$

(4 marks)

Answer

(b) Use the map to obtain a minimized expression for X

(4 marks)

Answer

(c) Draw the logic diagram for the minimized expression for X

(2 marks)

Answer

Q6. A silicon foundry(โรงหล่อ) factory has an airlock to prevents entry of polluted air into a cleanroom where wafers are processed as shown in Fig.3

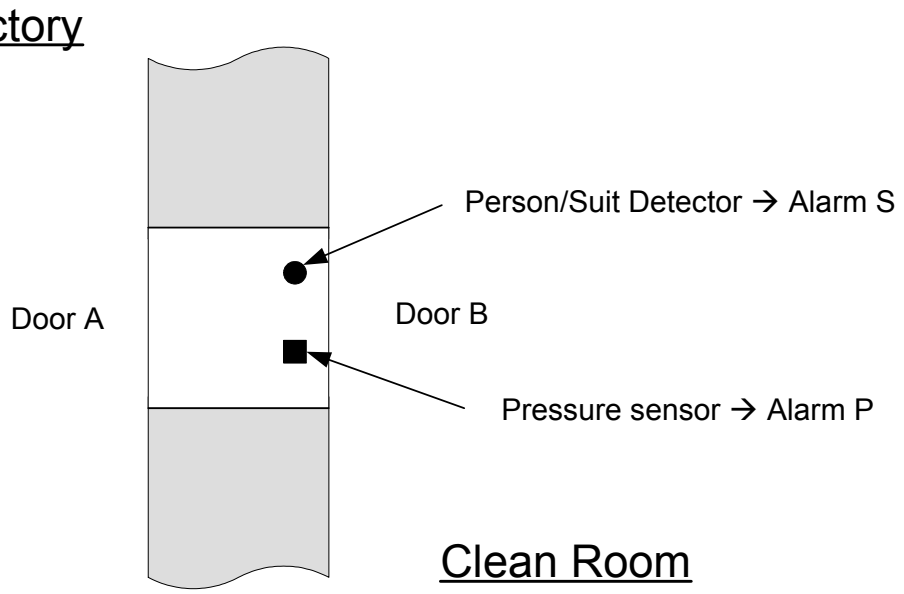


Fig.3

Personal are required to put on a cleanroom suit(สูท) when entering the cleanroom before opening Door B and are required to take it off before opening Door A.

Sensor on the person and suit cause an alarm S if these rules are broken.

A pressure sensor causes an alarm P if the airlock pressure rises above the cleanroom pressure.

Door A maybe opened if a person wishes to enter the airlock from the factory and Door B is closed and there is not a person already in the airlock.

Door B maybe opened if a person wishes to enter the airlock from the cleanroom and Door A is closed and there is not a person already in the airlock.

A person in the airlock may open door A without a suit or Door B with a suit.

Suit alarm S is activated if a person in the airlock tries to open Door A with a suit or Door B without a suit.

Pressure alarm P is activated if the pressure in the airlock rises above the pressure in the cleanroom.

(a) Develop a logic to open and close Doors A, B (8 marks)

Answer

(b) Discuss the use of alarms S and P (2 marks)

Answer

Q7. Fig. 4 represents a multiplier circuit that takes two-bit binary numbers x_1x_0 and y_1y_0 and produces an output binary number $z_3z_2z_1z_0$ that is equal to arithmetic product of the two input numbers (14 marks)

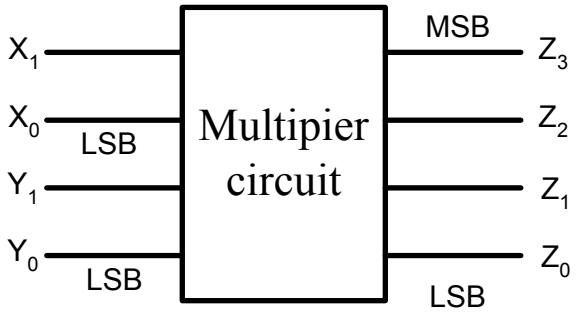


Fig. 4

(a) Design the logic circuit for the multiplier.

Answer

(b) Draw the logic diagram by using only NAND gate for output Z1 of Q7. (a) (6 marks)

Appendix

FAIRCHILD SEMICONDUCTOR™

March 1998

DM74LS08
Quad 2-Input AND Gates

General Description

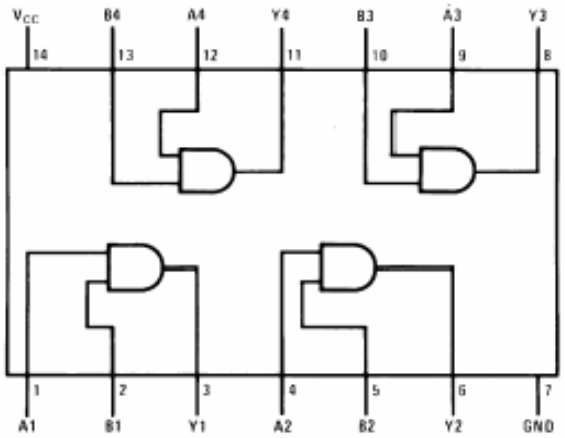
This device contains four independent gates each of which performs the logic AND function.

Features

- Alternate Military/Aerospace device (54LS08) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 54LS08DMQB, 54LS08FMQB, 54LS08LMQB, DM54LS08J, DM54LS08W, DM74LS08M or DM74LS08N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V	DM54LS and 54LS	−55°C to +125°C
Input Voltage	7V	DM74LS	0°C to +70°C
Operating Free Air Temperature Range		Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS08			DM74LS08			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			2.4	4.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			4.4	8.8	mA

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	5	18	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

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