

ชื่อ-สกุล.....รหัส.....

มหาวิทยาลัยสงขลานครินทร์

คณะวิศวกรรมศาสตร์



สอบปลายภาค: ภาคการศึกษาที่ 1

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ชื่อวิชา: Microprocessor Architecture and System design

อ่านรายละเอียดของข้อสอบ และคำแนะนำให้เข้าใจก่อนเริ่มทำข้อสอบ

เวลา: 3 ชั่วโมง (180 นาที)

รายละเอียดของข้อสอบ: ข้อสอบมีทั้งหมด 15 หน้า

- เป็นกระดาษคำถามจำนวน 7 หน้า
- เป็น Datasheet จำนวน 8 หน้า

อนุญาต: เครื่องเขียนต่างๆ เช่น ปากกา หรือดินสอ

ไม่อนุญาต: หนังสือและสมุดโน้ตใดๆ เข้าห้องสอบ

คำสั่ง:

- ให้ทำทุกข้อ
- คำตอบทั้งหมดจะต้องเขียนลงในข้อสอบ
- เขียนชื่อและรหัสให้ชัดเจนในข้อสอบทุกแผ่น แผ่นใดไม่เขียนหรือเขียนไม่ครบจะถูกหักคะแนน **1** คะแนน
- คำตอบส่วนใดอ่านไม่ออก จะถือว่าคำตอบนั้นผิด
- อ่านคำสั่งเพิ่มเติมในแต่ละข้อให้ชัดเจน
- ทุจริตในการสอบมีโทษขั้นต่ำปรับตกในรายวิชานั้นและพักการเรียน 1 ภาคการศึกษา โทษสูงสุดให้ออก

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1. จงอธิบายหน้าที่การทำงานของขา MCS-51 ต่อไปนี้ (5 คะแนน)

ALE.....

PSEN.....

RD.....

WR.....

EA.....

RST.....

P0.....

P2.....

P3.....

VSS.....

2. จงเปรียบเทียบคุณสมบัติของ MCS-51 กับ Z80 ในแง่ของ

2.1 ขนาดของหน่วยความจำที่สามารถอ้างถึงได้(2 คะแนน).....

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2.2 รูปแบบการจัดการอินพุตเอาต์พุต(2 คะแนน).....

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2.3 ความเร็วในการทำงาน(2 คะแนน).....

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2.4 ความยืดหยุ่นในการนำไปใช้งาน(2 คะแนน).....

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3. จงออกแบบระบบหน่วยความจำภายนอกของ MCS-51 โดยต่อกับหน่วยความจำอีพ롬ขนาด 32 กิโลไบต์ จำนวน 2 ตัว และหน่วยความจำสแตติกแรมขนาดตัวละ 8 กิโลไบต์ จำนวน 6 ตัว ให้เขียน schematic diagram ของวงจร พร้อมทั้งเขียน memory map ของระบบมาด้วย (15 คะแนน)

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4. จงออกแบบวงจรเพิ่มขยายพอร์ตของ MCS-51 เพื่อทำการต่อกับสวิทช์จำนวน 16 ตัว และแอลอีดีจำนวน 8 ตัว เข้ากับระบบไมโครโพรเซสเซอร์ซึ่งมีหน่วยความจำภายนอกเป็นสแตติกแรมขนาดเท่ากับ 32 กิโลไบต์ อยู่ที่ตำแหน่งแอดเดรส 0000-BFFFH (10 คะแนน)

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อ.ปัญญาศ ไชยกาฬ
ผู้ออกข้อสอบ

MCS[®]-51 INSTRUCTION SET

Table 10. 8051 Instruction Set Summary

Interrupt Response Time: Refer to Hardware Description Chapter.						
Instructions that Affect Flag Settings ⁽¹⁾						
Instruction	Flag			Instruction	Flag	
	C	OV	AC		C	OV
ADD	X	X	X	CLR C	O	
ADDC	X	X	X	CPLC	X	
SUBB	X	X	X	ANL C,bit	X	
MUL	O	X		ANL C,bit	X	
DIV	O	X		ORL C,bit	X	
DA	X			ORL C,bit	X	
RRC	X			MOV C,bit	X	
RLC	X			CJNE	X	
SETB C	1					

(1)Note that operations on SFR byte address 208 or bit addresses 209-215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

Note on instruction set and addressing modes:

- Rn — Register R7-R0 of the currently selected Register Bank.
- direct — 8-bit internal data location's address. This could be an Internal Data RAM location (0-127) or a SFR [i.e., I/O port, control register, status register, etc. (128-255)].
- @Ri — 8-bit internal data RAM location (0-255) addressed indirectly through register R1 or R0.
- #data — 8-bit constant included in instruction.
- #data 16 — 16-bit constant included in instruction.
- addr 16 — 16-bit destination address. Used by LCALL & LJMP. A branch can be anywhere within the 64K-byte Program Memory address space.
- addr 11 — 11-bit destination address. Used by ACALL & AJMP. The branch will be within the same 2K-byte page of program memory as the first byte of the following instruction.
- rel — Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is -128 to +127 bytes relative to first byte of the following instruction.
- bit — Direct Addressed bit in Internal Data RAM or Special Function Register.

Mnemonic	Description	Byte	Oscillator Period
ARITHMETIC OPERATIONS			
ADD A,Rn	Add register to Accumulator	1	12
ADD A,direct	Add direct byte to Accumulator	2	12
ADD A,@Ri	Add indirect RAM to Accumulator	1	12
ADD A,#data	Add immediate data to Accumulator	2	12
ADDC A,Rn	Add register to Accumulator with Carry	1	12
ADDC A,direct	Add direct byte to Accumulator with Carry	2	12
ADDC A,@Ri	Add indirect RAM to Accumulator with Carry	1	12
ADDC A,#data	Add immediate data to Acc with Carry	2	12
SUBB A,Rn	Subtract Register from Acc with borrow	1	12
SUBB A,direct	Subtract direct byte from Acc with borrow	2	12
SUBB A,@Ri	Subtract indirect RAM from ACC with borrow	1	12
SUBB A,#data	Subtract immediate data from Acc with borrow	2	12
INC A	Increment Accumulator	1	12
INC Rn	Increment register	1	12
INC direct	Increment direct byte	2	12
INC @Ri	Increment direct RAM	1	12
DEC A	Decrement Accumulator	1	12
DEC Rn	Decrement Register	1	12
DEC direct	Decrement direct byte	2	12
DEC @Ri	Decrement indirect RAM	1	12

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Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic	Description	Byte	Oscillator Period
ARITHMETIC OPERATIONS (Continued)			
INC DPTR	Increment Data Pointer	1	24
MUL AB	Multiply A & B	1	48
DIV AB	Divide A by B	1	48
DA A	Decimal Adjust Accumulator	1	12
LOGICAL OPERATIONS			
ANL A,Rn	AND Register to Accumulator	1	12
ANL A,direct	AND direct byte to Accumulator	2	12
ANL A,@Ri	AND indirect RAM to Accumulator	1	12
ANL A,#data	AND immediate data to Accumulator	2	12
ANL direct,A	AND Accumulator to direct byte	2	12
ANL direct,#data	AND immediate data to direct byte	3	24
ORL A,Rn	OR register to Accumulator	1	12
ORL A,direct	OR direct byte to Accumulator	2	12
ORL A,@Ri	OR indirect RAM to Accumulator	1	12
ORL A,#data	OR immediate data to Accumulator	2	12
ORL direct,A	OR Accumulator to direct byte	2	12
ORL direct,#data	OR immediate data to direct byte	3	24
XRL A,Rn	Exclusive-OR register to Accumulator	1	12
XRL A,direct	Exclusive-OR direct byte to Accumulator	2	12
XRL A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	12
XRL A,#data	Exclusive-OR immediate data to Accumulator	2	12
XRL direct,A	Exclusive-OR Accumulator to direct byte	2	12
XRL direct,#data	Exclusive-OR immediate data to direct byte	3	24
CLR A	Clear Accumulator	1	12
CPL A	Complement Accumulator	1	12

Mnemonic	Description	Byte	Oscillator Period
LOGICAL OPERATIONS (Continued)			
RL A	Rotate Accumulator Left	1	12
RLC A	Rotate Accumulator Left through the Carry	1	12
RR A	Rotate Accumulator Right	1	12
RRC A	Rotate Accumulator Right through the Carry	1	12
SWAP A	Swap nibbles within the Accumulator	1	12
DATA TRANSFER			
MOV A,Rn	Move register to Accumulator	1	12
MOV A,direct	Move direct byte to Accumulator	2	12
MOV A,@Ri	Move indirect RAM to Accumulator	1	12
MOV A,#data	Move immediate data to Accumulator	2	12
MOV Rn,A	Move Accumulator to register	1	12
MOV Rn,direct	Move direct byte to register	2	24
MOV Rn,#data	Move immediate data to register	2	12
MOV direct,A	Move Accumulator to direct byte	2	12
MOV direct,Rn	Move register to direct byte	2	24
MOV direct,direct	Move direct byte to direct	3	24
MOV direct,@Ri	Move indirect RAM to direct byte	2	24
MOV direct,#data	Move immediate data to direct byte	3	24
MOV @Ri,A	Move Accumulator to indirect RAM	1	12

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Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic	Description	Byte	Oscillator Period	Mnemonic	Description	Byte	Oscillator Period
DATA TRANSFER (Continued)				BOOLEAN VARIABLE MANIPULATION			
MOV	@Ri,direct	2	24	CLR	C	1	12
	Move direct byte to indirect RAM			CLR	bit	2	12
MOV	@Ri,#data	2	12	SETB	C	1	12
	Move immediate data to indirect RAM			SETB	bit	2	12
MOV	DPTR,#data16	3	24	CPL	C	1	12
	Load Data Pointer with a 16-bit constant				Carry		
MOVC	A,@A+DPTR	1	24	CPL	bit	2	12
	Move Code byte relative to DPTR to Acc				Complement direct bit		
MOVC	A,@A+PC	1	24	ANL	C,bit	2	24
	Move Code byte relative to PC to Acc				AND direct bit to CARRY		
MOVX	A,@Ri	1	24	ANL	C,/bit	2	24
	Move External RAM (8-bit addr) to Acc				AND complement of direct bit to Carry		
MOVX	A,@DPTR	1	24	ORL	C,bit	2	24
	Move External RAM (16-bit addr) to Acc				OR direct bit to Carry		
MOVX	@Ri,A	1	24	ORL	C,/bit	2	24
	Move Acc to External RAM (8-bit addr)				OR complement of direct bit to Carry		
MOVX	@DPTR,A	1	24	MOV	C,bit	2	12
	Move Acc to External RAM (16-bit addr)				Move direct bit to Carry		
PUSH	direct	2	24	MOV	bit,C	2	24
	Push direct byte onto stack				Move Carry to direct bit		
POP	direct	2	24	JC	rel	2	24
	Pop direct byte from stack				Jump if Carry is set		
XCH	A,Rn	1	12	JNC	rel	2	24
	Exchange register with Accumulator				Jump if Carry not set		
XCH	A,direct	2	12	JB	bit,rel	3	24
	Exchange direct byte with Accumulator				Jump if direct Bit is set		
XCH	A,@Ri	1	12	JNB	bit,rel	3	24
	Exchange indirect RAM with Accumulator				Jump if direct Bit is Not set		
XCHD	A,@Ri	1	12	JBC	bit,rel	3	24
	Exchange low-order Digit indirect RAM with Acc				Jump if direct Bit is set & clear bit		
				PROGRAM BRANCHING			
				ACALL	addr11	2	24
					Absolute Subroutine Call		
				LCALL	addr16	3	24
					Long Subroutine Call		
				RET		1	24
					Return from Subroutine		
				RETI		1	24
					Return from interrupt		
				AJMP	addr11	2	24
					Absolute Jump		
				LJMP	addr16	3	24
					Long Jump		
				SJMP	rel	2	24
					Short Jump (relative addr)		

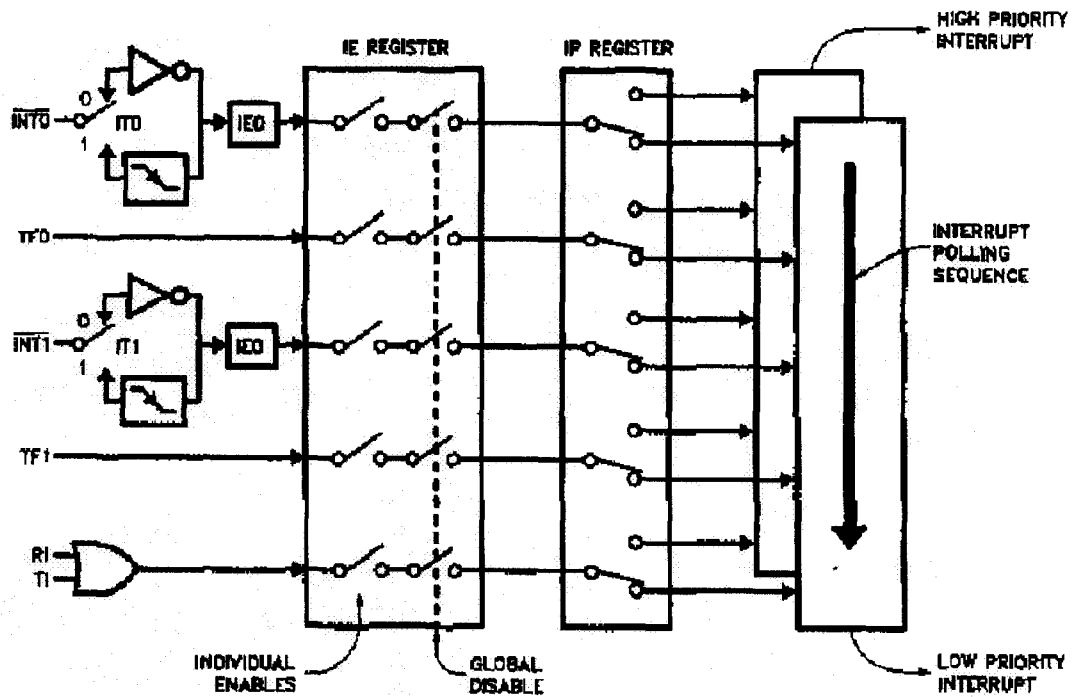
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Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic	Description	Byte	Oscillator Period	Mnemonic	Description	Byte	Oscillator Period
PROGRAM BRANCHING (Continued)				PROGRAM BRANCHING (Continued)			
JMP	@A + DPTR Jump indirect relative to the DPTR	1	24	CJNE	Rn, #data, rel Compare immediate to register and Jump if Not Equal	3	24
JZ	rel Jump if Accumulator is Zero	2	24	CJNE	@Ri, #data, rel Compare immediate to indirect and Jump if Not Equal	3	24
JNZ	rel Jump if Accumulator is Not Zero	2	24	DJNZ	Rn, rel Decrement register and Jump if Not Zero	2	24
CJNE	A, direct, rel Compare direct byte to Acc and Jump if Not Equal	3	24	DJNZ	direct, rel Decrement direct byte and Jump if Not Zero	3	24
CJNE	A, #data, rel Compare immediate to Acc and Jump if Not Equal	3	24	NOF	No Operation	1	12

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PSW Structure



SFR MEMORY MAP

8 Bytes

F8									FF
F0	B								F7
E8									EF
E0	ACC								E7
D8									DF
D0	PSW								D7
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2			CF
C0									C7
B8	IP								BF
B0	P3								B7
A8	IE								AF
A0	P2								A7
98	SCON	SBUF							9F
90	P1								97
88	TCON	TMOD	TL0	TL1	TH0	TH1			8F
80	P0	SP	DPL	DPH				PCON	87

↑
Bit
Addressable

Figure 5

PCON: POWER CONTROL REGISTER. NOT BIT ADDRESSABLE.

SMOD	—	—	—	GF1	GF0	PD	IDL
------	---	---	---	-----	-----	----	-----

SMOD Double baud rate bit. If Timer 1 is used to generate baud rate and SMOD = 1, the baud rate is doubled when the Serial Port is used in modes 1, 2, or 3.

- Not implemented, reserved for future use.*
- Not implemented, reserved for future use.*
- Not implemented, reserved for future use.*

GF1 General purpose flag bit.

GF0 General purpose flag bit.

PD Power Down bit. Setting this bit activates Power Down operation in the 80C51BH. (Available only in CHMOS).

IDL Idle Mode bit. Setting this bit activates Idle Mode operation in the 80C51BH. (Available only in CHMOS).

Interrupt Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI & TI	0023H
TF2 & EXF2	002BH

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IP: INTERRUPT PRIORITY REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt has a lower priority and if the bit is 1 the corresponding interrupt has a higher priority.

—	—	PT2	PS	PT1	PX1	PT0	PX0
---	---	-----	----	-----	-----	-----	-----

- IP. 7 Not implemented, reserved for future use.*
- IP. 6 Not implemented, reserved for future use.*
- PT2 IP. 5 Defines the Timer 2 interrupt priority level (8052 only).
- PS IP. 4 Defines the Serial Port interrupt priority level.
- PT1 IP. 3 Defines the Timer 1 interrupt priority level.
- PX1 IP. 2 Defines External Interrupt 1 priority level.
- PT0 IP. 1 Defines the Timer 0 interrupt priority level.
- PX0 IP. 0 Defines the External Interrupt 0 priority level.

TCON: TIMER/COUNTER CONTROL REGISTER. BIT ADDRESSABLE.

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
-----	-----	-----	-----	-----	-----	-----	-----

- TF1 TCON. 7 Timer 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as processor vectors to the interrupt service routine.
- TR1 TCON. 6 Timer 1 run control bit. Set/cleared by software to turn Timer/Counter 1 ON/OFF.
- TF0 TCON. 5 Timer 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as processor vectors to the service routine.
- TR0 TCON. 4 Timer 0 run control bit. Set/cleared by software to turn Timer/Counter 0 ON/OFF.
- IE1 TCON. 3 External Interrupt 1 edge flag. Set by hardware when External Interrupt edge is detected. Cleared by hardware when interrupt is processed.
- IT1 TCON. 2 Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered External Interrupt.
- IE0 TCON. 1 External Interrupt 0 edge flag. Set by hardware when External Interrupt edge detected. Cleared by hardware when interrupt is processed.
- IT0 TCON. 0 Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered External Interrupt.

TMOD: TIMER/COUNTER MODE CONTROL REGISTER. NOT BIT ADDRESSABLE.

GATE	C/T	M1	M0	GATE	C/T	M1	M0
------	-----	----	----	------	-----	----	----

TIMER 1

TIMER 0

- GATE When TRx (in TCON) is set and GATE = 1, TIMER/COUNTERx will run only while INTx pin is high (hardware control). When GATE = 0, TIMER/COUNTERx will run only while TRx = 1 (software control).
- C/T Timer or Counter selector. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin).
- M1 Mode selector bit. (NOTE 1)
- M0 Mode selector bit. (NOTE 1)

NOTE 1:

M1	M0	Operating Mode
0	0	13-bit Timer (MCS-48 compatible)
0	1	16-bit Timer/Counter
1	0	8-bit Auto-Reload Timer/Counter
1	1	3 (Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits, TH0 is an 8-bit Timer and is controlled by Timer 1 control bits.
1	1	3 (Timer 1) Timer/Counter 1 stopped.

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SCON: SERIAL PORT CONTROL REGISTER. BIT ADDRESSABLE.

SM0	SM1	SM2	REN	TB8	RB8	TI	RI
-----	-----	-----	-----	-----	-----	----	----

- SM0** SCON. 7 Serial Port mode specifier. (NOTE 1).
SM1 SCON. 6 Serial Port mode specifier. (NOTE 1).
SM2 SCON. 5 Enables the multiprocessor communication feature in modes 2 & 3. In mode 2 or 3, if SM2 is set to 1 then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In mode 0, SM2 should be 0. (See Table 9).
REN SCON. 4 Set/Cleared by software to Enable/Disable reception.
TB8 SCON. 3 The 9th bit that will be transmitted in modes 2 & 3. Set/Cleared by software.
RB8 SCON. 2 In modes 2 & 3, is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI SCON. 1 Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes. Must be cleared by software.
RI SCON. 0 Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes (except see SM2). Must be cleared by software.

NOTE 1:

SM0	SM1	Mode	Description	Baud Rate
0	0	0	SHIFT REGISTER	Fosc./12
0	1	1	8-Bit UART	Variable
1	0	2	9-Bit UART	Fosc./64 OR Fosc./32
1	1	3	9-Bit UART	Variable

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	—	ET2	ES	ET1	EX1	ET0	EX0
----	---	-----	----	-----	-----	-----	-----

- EA** IE.7 Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
— IE.6 Not implemented, reserved for future use.*
ET2 IE.5 Enable or disable the Timer 2 overflow or capture interrupt (8052 only).
ES IE.4 Enable or disable the serial port interrupt.
ET1 IE.3 Enable or disable the Timer 1 overflow interrupt.
EX1 IE.2 Enable or disable External Interrupt 1.
ET0 IE.1 Enable or disable the Timer 0 overflow interrupt.
EX0 IE.0 Enable or disable External Interrupt 0.

*User software should not write 1s to reserved bits. These bits may be used in future MCS-51 products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1.

Baud Rate	fosc	SMOD	Timer 1		
			C/T	Mode	Reload Value
Mode 0 Max: 1 MHz	12 MHz	X	X	X	X
Mode 2 Max: 375K	12 MHz	1	X	X	X
Modes 1, 3: 62.5K	12 MHz	1	0	2	FFH
19.2K	11.059 MHz	1	0	2	FDH
9.6K	11.059 MHz	0	0	2	FDH
4.8K	11.059 MHz	0	0	2	FAH
2.4K	11.059 MHz	0	0	2	F4H
1.2K	11.059 MHz	0	0	2	E8H
137.5	11.986 MHz	0	0	2	1DH
110	6 MHz	0	0	2	72H
110	12 MHz	0	0	1	FE8BH

Figure 15. Timer 1 Generated Commonly Used Baud Rates

Control Word of 8255

