ชื่อ _____ รหัส _____

**มหาวิทยาลัยสงขลานครินทร์**
**คณะวิศวกรรมศาสตร์**

การสอบปลายภาค ประจำภาคการศึกษาที่ 1 ปีการศึกษา 2547
วันที่ : 3 ตุลาคม 2547 เวลา : 13.30-16.30
วิชา : 240-333 Microcomputer interfacing and Applications ห้อง : A201

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<u>คำสั่ง</u>

- ข้อสอบมีทั้งหมด **9** ข้อ คะแนนเต็ม 40 คะแนน ให้นักศึกษาทำหมดทุกข้อ
- นำเอกสารหรือหนังสือเข้าห้องสอบได้
- นำเครื่องคิดเลขเข้าห้องสอบได้

คำแนะนำ

- อ่านข้อสอบและดูวงจรให้ละเอียด(โดยเฉพาะชนิดของอุปกรณ์ที่ใช้ในวงจร)ก่อนเริ่มทำข้อสอบ
- เขียนคำตอบให้ชัดเจนด้วยลายมือที่ได้อ่านง่าย

ทุจริตปรับโทษต่ำสุดปรับตกวิชานี้และพักการเรียน 1 ภาคการศึกษา โทษสูงสุดไล่ออก

ชื่อ _____ รหัส _____

1 นายสมชายซื้อมัลติมิเตอร์มาใช้งานตัวหนึ่ง นายสมชายพบว่ามัลติมิเตอร์ตัวนี้สามารถต่อกับพอร์ทอนุกรมได้ โดยรูปแบบต้องใช้ความเร็วในการรับส่ง 9600 bit/sec รูปแบบข้อมูล 7 บิต 1 stop bit และมีการตรวจสอบ even parity การส่งข้อมูลไปควบคุมมัลติมิเตอร์ต้องส่งไป 2 ไบต์ ไบต์แรกเป็นการส่งคำสั่งหลัก ไบต์สองเป็นการส่งคำสั่งย่อย ข้อมูลที่ส่งออกจากมัลติมิเตอร์ 1 ชุดมี 3 ไบต์ เป็นข้อมูลที่มัลติมิเตอร์วัดได้

จากคำอธิบายดังกล่าวจงตอบคำถามต่อไปนี้ (10 คะแนน)

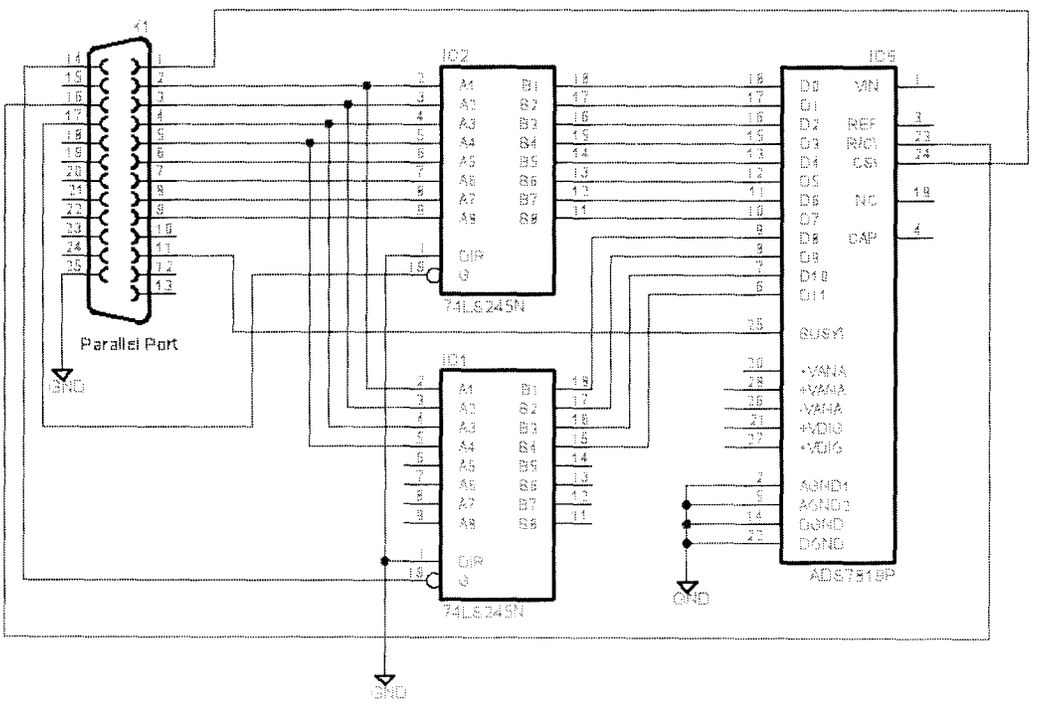
1.1 นายสมชายต้องเขียนโปรแกรมกำหนดความเร็วในการรับส่ง 9600 bit/sec รูปแบบข้อมูล 7 บิต 1 stop bit และมีการตรวจสอบ even parity โดยใช้ภาษา C อย่างไรเมื่อนายสมชายต้องการใช้ com2 (4 คะแนน)

1.2 นายสมชายต้องเขียนโปรแกรมส่งข้อมูล โดยใช้ภาษา C อย่างไร ? (3 คะแนน)

ชื่อ _____ รหัส _____

1.3 นายสมชายต้องเขียนโปรแกรมรับข้อมูล โดยใช้ภาษา C อย่างไร ? (3 คะแนน)

2 จากวงจรในรูปที่ 1 ให้นักศึกษาเขียนโปรแกรมโดยใช้ภาษา C เพื่อสั่งให้ A/D ทำการแปลงสัญญาณอนาลอกเป็นดิจิตอลและอ่านข้อมูลที่แปลงเข้ามา (10 คะแนน)

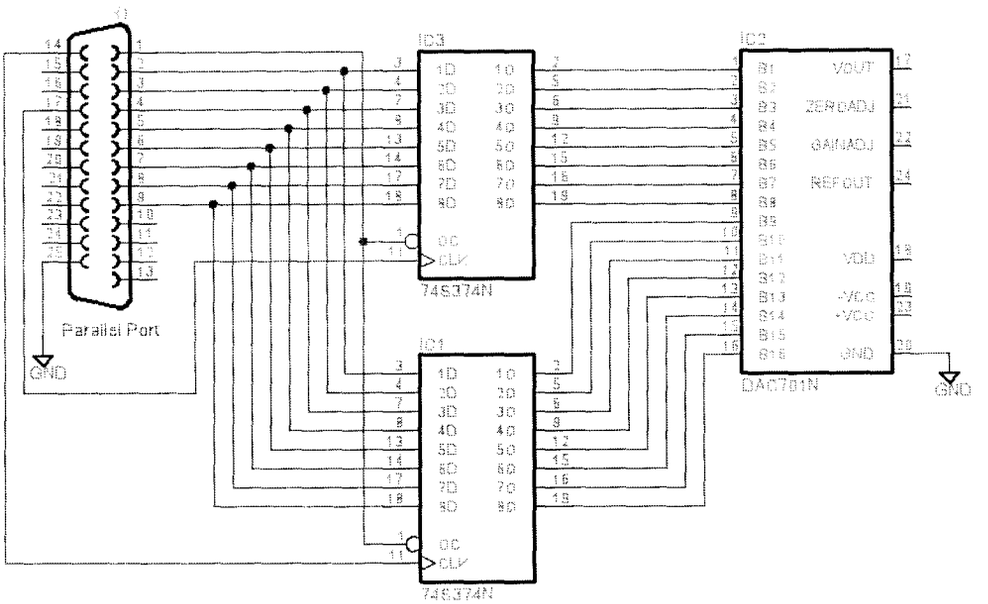



รูปที่ 1 วงจรการต่อ A/D ผ่านทาง parallel port

ชื่อ _____ รหัส _____

ชื่อ _____ รหัส _____

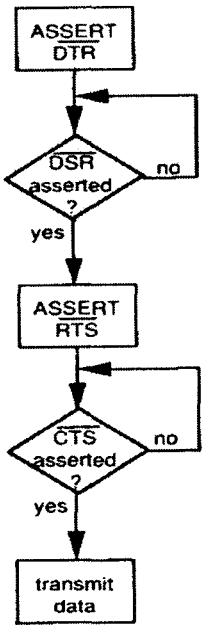
3 จากวงจรในรูปที่ 2 ให้นักศึกษาเขียนโปรแกรมโดยใช้ภาษา C เพื่อสั่งให้ D/A ทำการแปลงสัญญาณดิจิตอลเป็นอนาลอก (5 คะแนน)




รูปที่ 2 วงจรการต่อ D/A ผ่านทาง parallel port

ชื่อ _____ รหัส _____

4 จงเขียนโปรแกรมด้วยภาษา C ติดต่อกับโมเด็มผ่านทาง com1 ตามโฟลว์ชาร์ตในรูปที่ 3 (5 คะแนน)




รูปที่ 3 โฟลว์ชาร์ตการติดต่อกับโมเด็ม

ชื่อ _____ รหัส _____

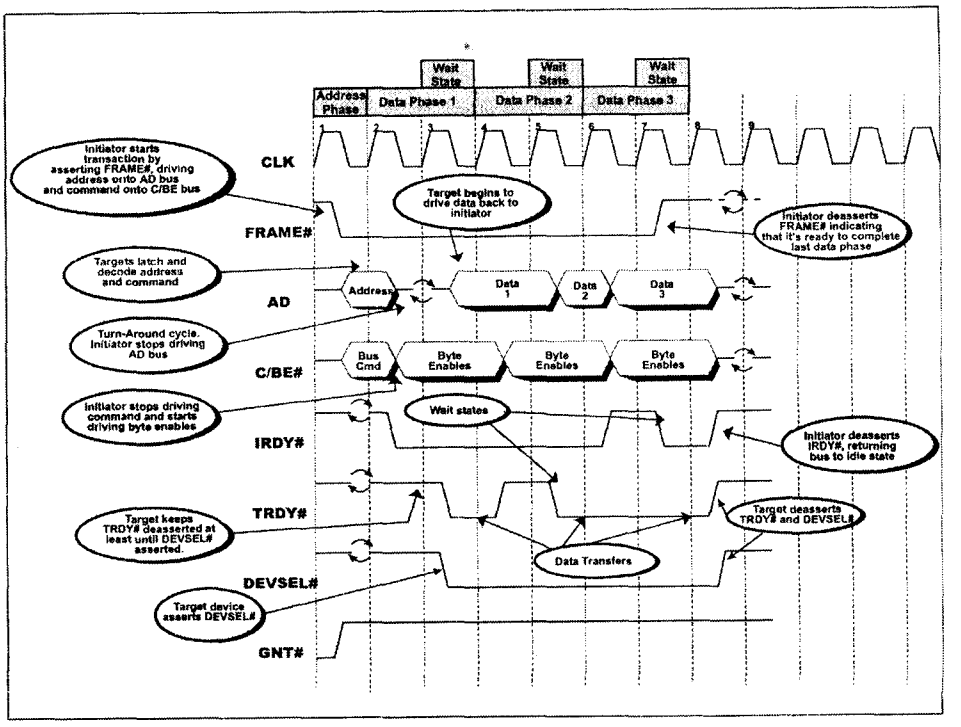
5 จงอธิบายการทำ arbitration ระหว่าง master เพื่อเข้าใช้งาน bus (2 คะแนน)

6 จงอธิบายการอ่านค่าเวลาจาก Real time clock ของ PC (2 คะแนน)

7 สัญญาณใดบ้างของ PCI bus ซึ่งใช้ในการทำ wait state (1 คะแนน)

ชื่อ _____ รหัส _____

8 จงอธิบาย read transfer แบบ Burst read ตามรูปที่ 4 (3 คะแนน)

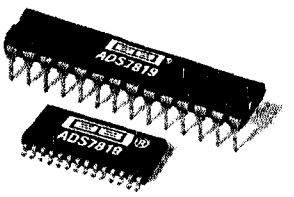



รูปที่ 4 Burst read cycle

ชื่อ _____ รหัส _____

9. จงอธิบายวิธีการทำอินเทอร์รัพท์แบบ MSI บน PCI bus (2 คะแนน)

BURR-BROWN®




# ADS7819

# 12-Bit 800kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

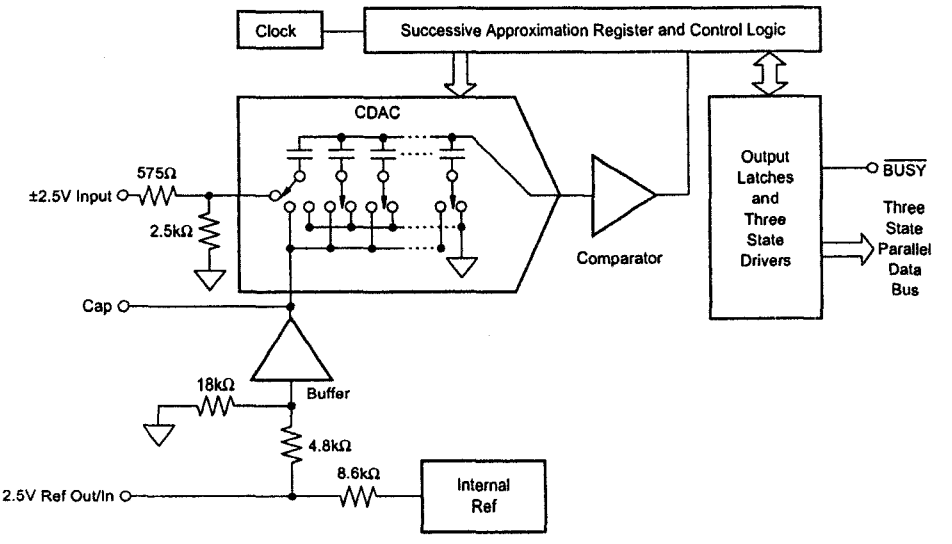
- 1.25µs THROUGHPUT TIME
- STANDARD ±2.5V INPUT RANGE
- 70dB min SINAD WITH 250kHz INPUT
- ±3/4 LSB max INL AND ±1 LSB max DNL
- INTERNAL REFERENCE
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- PARALLEL DATA w/ LATCHES
- 28-PIN 0.3" PDIP AND SOIC

## DESCRIPTION

The ADS7819 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7819 is specified at an 800kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide a ±2.5V input range and inherent overvoltage protection up to ±25V.

The 28-pin ADS7819 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.

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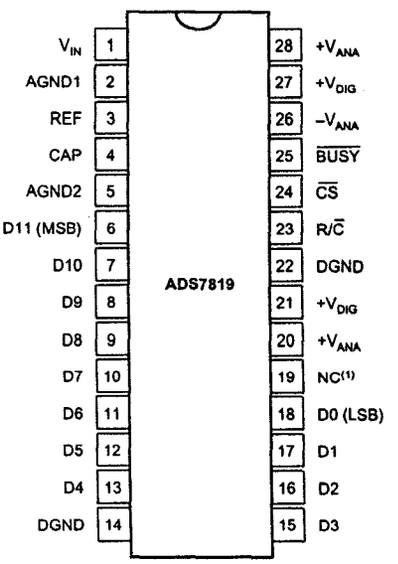
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132


PDS-1193C
Printed in U.S.A. February, 1995

## PIN ASSIGNMENTS

| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{IN}$ | | Analog Input. Connect via 50Ω to analog input. Full-scale input range is ±2.5V. |
| 2 | AGND1 | | Analog Ground. Used internally as ground reference point. Minimal current flow. |
| 3 | REF | | Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, decouple to ground with a 0.1µF ceramic capacitor. |
| 4 | CAP | | Reference Buffer Output. 10µF tantalum capacitor to ground. Nominally +2V. |
| 5 | AGND2 | | Analog Ground. |
| 6 | D11 (MSB) | O | Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 7 | D10 | O | Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 8 | D9 | O | Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 9 | D8 | O | Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 10 | D7 | O | Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 11 | D6 | O | Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress |
| 12 | D5 | O | Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 13 | D4 | O | Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 14 | DGND | | Digital Ground. |
| 15 | D3 | O | Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 16 | D2 | O | Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 17 | D1 | O | Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 18 | D0 (LSB) | O | Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 19 | | | Not internally connected. |
| 20 | $+V_{ANA}$ | | Analog Positive Supply Input. Nominally +5V. Connect directly to pins 21, 27 and 28. |
| 21 | $+V_{DIG}$ | | Digital Supply Input. Nominally +5V. Connect directly to pins 20, 27 and 28. |
| 22 | DGND | | Digital ground. |
| 23 | R/$\overline{C}$ | I | Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW and no conversion in progress, a rising edge on R/$\overline{C}$ enables the output data bits. |
| 24 | $\overline{CS}$ | I | Chip Select. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH and no conversion in progress, a falling edge on $\overline{CS}$ will enable the output data bits. |
| 25 | $\overline{BUSY}$ | O | Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data. |
| 26 | $-V_{ANA}$ | | Analog Negative Supply Input. Nominally –5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors. |
| 27 | $+V_{DIG}$ | | Digital Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 28. |
| 28 | $+V_{ANA}$ | | Analog Positive Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 27, and decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors. |

## PIN CONFIGURATION




NOTE: (1) Not Internally Connected.

## BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7819. Taking R/$\overline{C}$ (pin 23) LOW for 40ns will initiate a conversion. $\overline{BUSY}$ (pin 25) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on D11 (pin 6). $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

| $\overline{CS}$ | R/$\overline{C}$ | $\overline{BUSY}$ | OPERATION |
|---|---|---|---|
| 1 | X | X | None. Databus in Hi-Z state. |
| ↓ | 0 | 1 | Initiates conversion. Databus remains in Hi-Z state. |
| 0 | ↓ | 1 | Initiates conversion. Databus enters Hi-Z state. |
| 0 | 1 | ↑ | Conversion completed. Valid data from the most recent conversion on the databus. |
| ↓ | 1 | 1 | Enables databus with valid data from the most recent conversion. |
| ↓ | 1 | 0 | Conversion in progress. Databus in Hi-Z state, enabled when the conversion is completed. |
| 0 | ↑ | 0 | Conversion in progress. Databus in Hi-Z state, enabled when the conversion is completed. |
| 0 | 0 | ↑ | Conversion completed. Valid data from the most recent conversion in the output register but the output pins D11-D0 are tri-stated. |
| X | X | 0 | New convert commands ignored. Conversion in progress. |

Table I. Control Line Functions for 'read' and 'convert'.

The ADS7819 will begin tracking the input signal at the end of the conversion. Allowing 1.25µs between convert commands assures accurate acquisition of a new signal.

## STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 24) and R/$\overline{C}$ (pin 23) LOW for a minimum of 40ns puts the sample/hold of the ADS7819 in the hold state and starts a conversion. $\overline{BUSY}$ (pin 25) will go LOW and stay LOW until the conversion is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored.

The ADS7819 will begin tracking the input signal at the end of the conversion. Allowing 1.25µs between convert commands assures accurate acquisition of a new signal. Refer to Table I for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 2 and 3 for timing parameters.

| DESCRIPTION | ANALOG VALUE | DIGITAL OUTPUT | |
|---|---|---|---|
| Full Scale Range | ±2.5V | BINARY TWO'S COMPLEMENT | |
| Least Significant Bit (LSB) | 1.22mV | BINARY CODE | HEX CODE |
| +Full Scale (2.5V – 1LSB) | 2.499V | 0111 1111 1111 | 7FF |
| Midscale | 0V | 0000 0000 0000 | 000 |
| One LSB below Midscale | –1.22mV | 1111 1111 1111 | FFF |
| –Full Scale | –2.5V | 1000 0000 0000 | 800 |

TABLE II. Ideal Input Voltages and Output Codes.

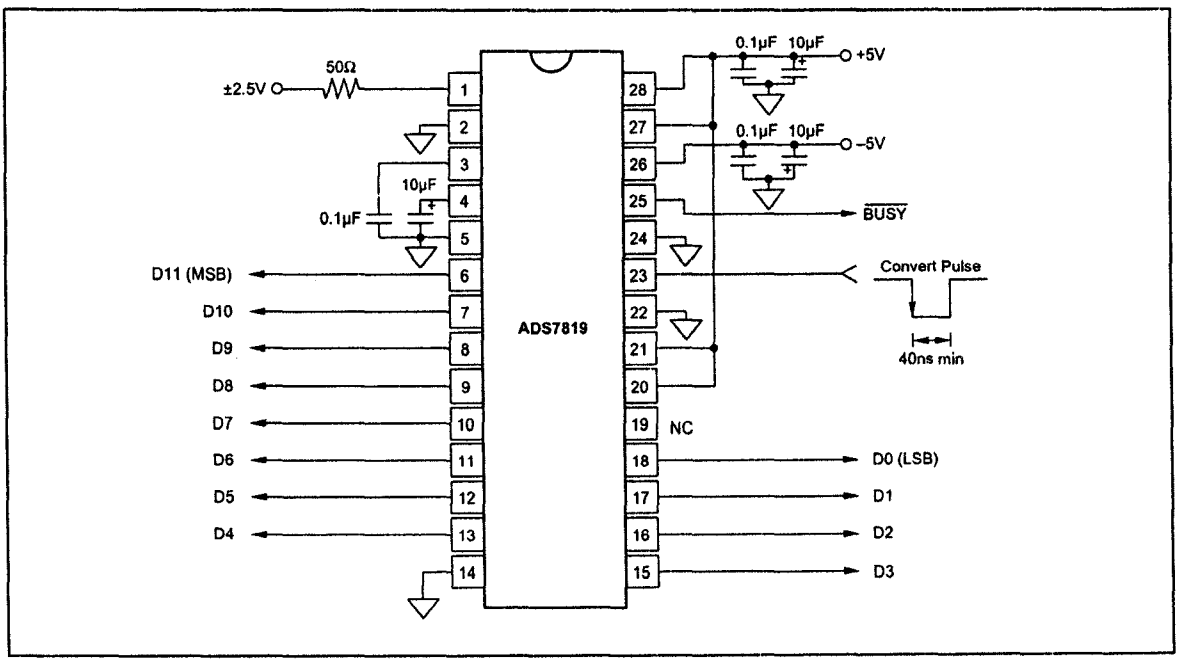



FIGURE 1. Basic Operation

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If it is critical that $\overline{CS}$ or R/$\overline{C}$ initiate the conversion, be sure the less critical input is LOW at least 10ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. Note that the parallel output will be active whenever R/$\overline{C}$ is HIGH and no conversion is in progress. See the **Reading Data** section and refer to Table I for control line functions for 'read' and 'convert' modes.

## READING DATA

The ADS7819 outputs full parallel data in Binary Two's Complement data format. The parallel output will be active when R/$\overline{C}$ (pin 23) is HIGH, $\overline{CS}$ (pin 24) is LOW, and no conversion is in progress. Any other combination will tri-state the parallel output. Valid conversion data can be read in a full parallel, 12-bit word on D11-D0 (pins 6-13 and 15-18). Refer to Table II for ideal output codes.

After the conversion is completed and the output registers have been updated, $\overline{BUSY}$ (pin 25) will go HIGH. Valid data from the most recent conversion will be available on D11-D0 (pins 6-13 and 15-18). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table III and Figures 2 and 3.

Note: For best performance, the external data bus connected to D11-D0 should not be active during a conversion. The switching noise of the external asynchronous data signals can cause digital feed through degrading the converter's performance.

The number of control lines can be reduced by tieing $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 2.

## INPUT RANGES

The ADS7819 has a ±2.5V input range. Figures 4a and 4b show the necessary circuit connections for the ADS7819 with and without external hardware trim. Offset and full scale error(1) specifications are tested and guaranteed with the 50Ω resistor shown in Figure 4b. This external resistor makes it possible to trim the offset ±12mV using a trim pot or trim DAC. This resistor may be left out if the offset and gain errors will be corrected in software or if they are negligible in regards to the particular application. See the **Calibration** section of the data sheet for details.

The nominal input impedance of 3.125kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet and the external 50Ω resistor. The input resistor divider network provides inherent over-voltage protection guaranteed to at least ±25V. The 50Ω, 1% resistor does not compromise the accuracy or drift of the converter. It has little influence relative to the internal resistors, and tighter tolerances are not required.

Note: The values shown for the internal resistors are for reference only. The exact values can vary by ±30%. This is true of all resistors internal to the ADS7819. Each resistive divider is trimmed so that the proper division is achieved.

NOTE: (1) Full scale error includes offset and gain errors and is measured at both +FS and –FS.

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_1$ | Convert Pulse Width | 40 | | | ns |
| $t_2$ | Data Valid Delay After Start of Conversion | | 965 | 1100 | ns |
| $t_3$ | $\overline{BUSY}$ Delay From Start of Conversion | | 70 | 125 | ns |
| $t_4$ | $\overline{BUSY}$ LOW | | 960 | 1085 | ns |
| $t_5$ | $\overline{BUSY}$ Delay After End of Conversion | | 90 | | ns |
| $t_6$ | Aperture Delay | | 20 | | ns |
| $t_7$ | Conversion Time | | 940 | 1030 | ns |
| $t_8$ | Acquisition Time | | 180 | 220 | ns |
| $t_7$ & $t_8$ | Throughput Time | | 1120 | 1250 | ns |
| $t_9$ | Bus Relinquish Time | 10 | 50 | 83 | ns |
| $t_{10}$ | $\overline{BUSY}$ Delay After Data Valid | 20 | 65 | 100 | ns |
| $t_{11}$ | R/$\overline{C}$ to $\overline{CS}$ Setup Time | 10 | | | ns |
| $t_{12}$ | Time Between Conversions | 1250 | | | ns |
| $t_{13}$ | Bus Access Time | 10 | 30 | 62 | ns |

TABLE III. Timing Specifications ($T_{MIN}$ to $T_{MAX}$).

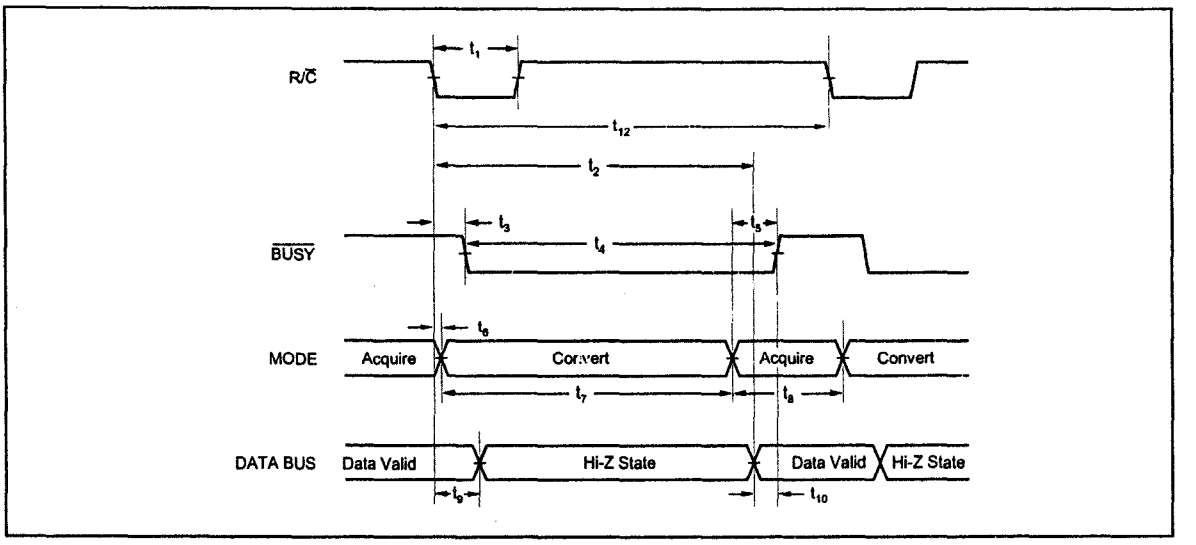



FIGURE 2. Conversion Timing with Outputs Enabled After Conversion ($\overline{CS}$ Tied Low).

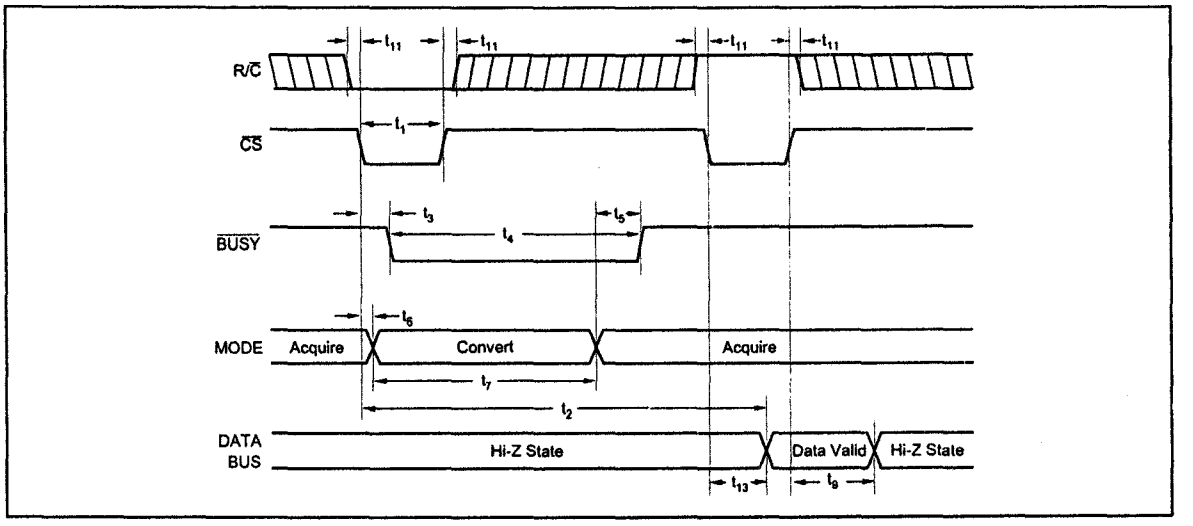



FIGURE 3. Using $\overline{CS}$ to Control Conversion and Read Timing.

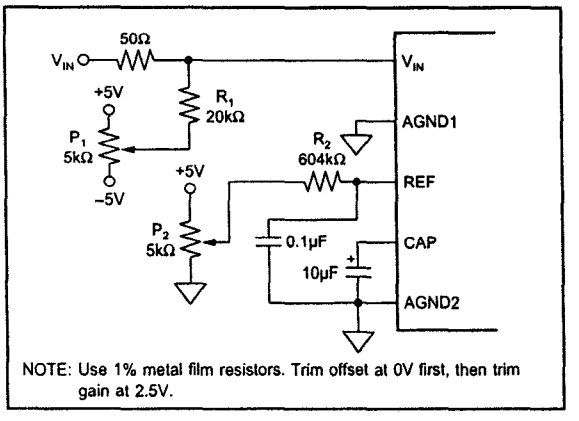



FIGURE 4a. Circuit Diagram With External Hardware Trim.

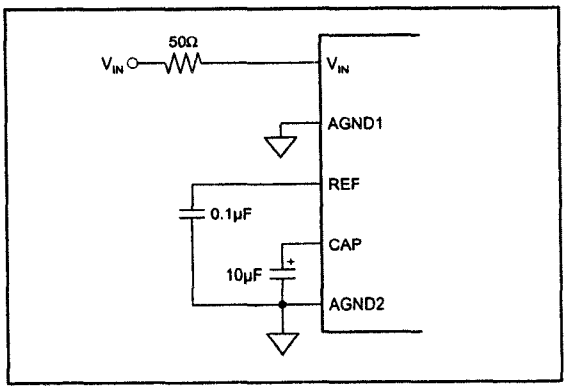



FIGURE 4b. Circuit Diagram Without External Hardware Trim.

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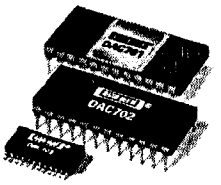


# DAC701
# DAC702
# DAC703

# Monolithic 16-Bit DIGITAL-TO-ANALOG CONVERTERS

## FEATURES

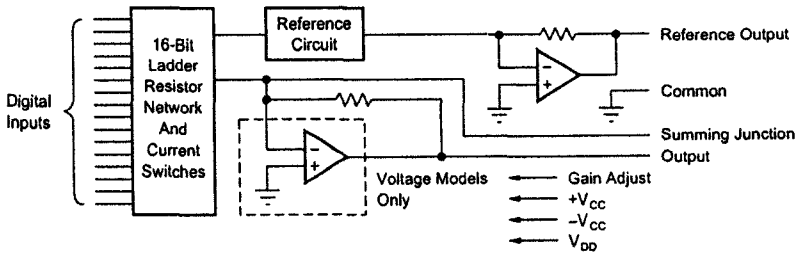
- $V_{OUT}$ AND $I_{OUT}$ MODELS
- HIGH ACCURACY:
  Linearity Error ±0.0015% of FSR max
  Differential Linearity Error ±0.003% of FSR max
- MONOTONIC (at 15 bits) OVER FULL SPECIFICATION TEMPERATURE RANGE
- PIN-COMPATIBLE WITH DAC70, DAC71, DAC72
- DUAL-IN-LINE PLASTIC AND HERMETIC CERAMIC AND SOIC

## DESCRIPTION

The DAC70X family comprise of complete 16-bit digital-to-analog converters that includes a precision buried-zener voltage reference and a low-noise, fast-settling output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 15-bit monotonicity over the entire specified temperature range, but also a maximum end-point linearity error of ±0.0015% of full-scale range. Total full-scale gain drift is limited to ±10ppm/°C maximum (LH and CH grades).

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V, ±10V, 0 to −2mA, and ±1mA are available.

These D/A converters are packaged in hermetic 24-pin ceramic side-brazed or molded plastic. The DIP-packaged parts are pin-compatible with the voltage and current output DAC71 and DAC72 model families. The DAC702 is also pin-compatible with the DAC70 model family. In addition, the DAC703 is offered in a 24-pin SOIC package for surface mount applications.

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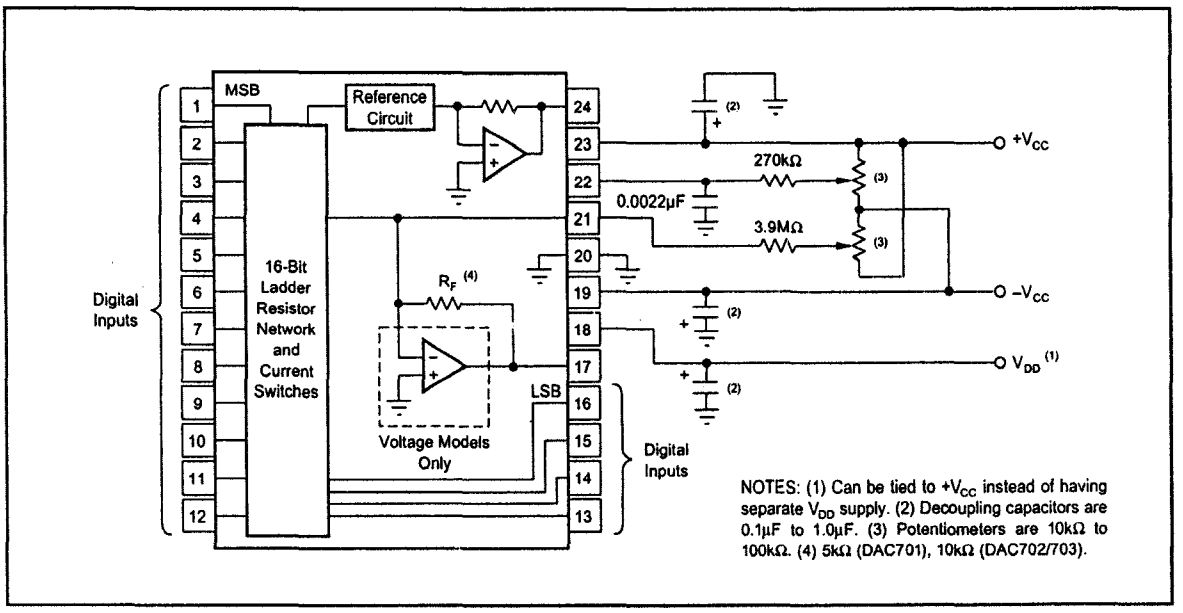
PDS-494M
Printed in U.S.A. March, 1998

## CONNECTION DIAGRAMS




NOTES: (1) Can be tied to +$V_{CC}$ instead of having separate $V_{DD}$ supply. (2) Decoupling capacitors are 0.1µF to 1.0µF. (3) Potentiometers are 10kΩ to 100kΩ. (4) 5kΩ (DAC701), 10kΩ (DAC702/703).

## PIN ASSIGNMENTS

| PIN # | ALL PACKAGES | |
|---|---|---|
| | DAC702 | DAC701/703 |
| 1 | Bit 1 (MSB) | Bit 1 (MSB) |
| 2 | Bit 2 | Bit 2 |
| 3 | Bit 3 | Bit 3 |
| 4 | Bit 4 | Bit 4 |
| 5 | Bit 5 | Bit 5 |
| 6 | Bit 6 | Bit 6 |
| 7 | Bit 7 | Bit 7 |
| 8 | Bit 8 | Bit 8 |
| 9 | Bit 9 | Bit 9 |
| 10 | Bit 10 | Bit 10 |
| 11 | Bit 11 | Bit 11 |
| 12 | Bit 12 | Bit 12 |
| 13 | Bit 13 | Bit 13 |
| 14 | Bit 14 | Bit 14 |
| 15 | Bit 15 | Bit 15 |
| 16 | Bit 16 (LSB) | Bit 16 (LSB) |
| 17 | $R_{FEEDBACK}$ | $V_{OUT}$ |
| 18 | $V_{DD}$ | $V_{DD}$ |
| 19 | $-V_{CC}$ | $-V_{CC}$ |
| 20 | Common | Common |
| 21 | $I_{OUT}$ | Summing Junction (Zero Adjust) |
| 22 | Gain Adjust | Gain Adjust |
| 23 | $+V_{CC}$ | $+V_{CC}$ |
| 24 | +6.3V Reference Output | +6.3V Reference Output |

## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| $+V_{CC}$ to Common | 0V, +18V |
| $-V_{CC}$ to Common | 0V, –18V |
| $V_{DD}$ to Common | 0V. +18V |
| Digital Data Inputs to Common | –1V, +18V |
| Reference Out to Common | Indefinite Short to Common |
| External Voltage Applied to $R_F$ (DAC702) | ±18V |
| External Voltage Applied to D/A Output (DAC701/703) | –5V to +5V |
| $V_{OUT}$ (DAC701/703) | Indefinite Short to Common |
| Power Dissipation | 1W |
| Storage Temperature | –60°C to +150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.