Department of Computer Engineering

Faculty of Engineering

Prince of Songkla University

Final Examination: Semester I — Academic Year: 2005

Date: 6 October 2005 — Time: 9:00-11:00

Subject: 240-440 VLSI System Design — Room: A400

คำสั่ง 1. ข้อสอบมีทั้งหมด 5 ข้อ ให้ทำทุกข้อ

2. อนุญาตให้นำโน๊ตขนาด A4 เข้าห้องสอบได้ 1 แผ่น

3. อนุญาตให้ใช้เครื่องคิดเลขได้ และทำข้อสอบด้วยดินสอหรือปากกา

ผู้ออกข้อสอบ ณัฏฐา จินดาเพ็ชร์

1. 4-input NAND gates in Fig 1(a) and 1(b) have input capacitance of 10 units on each input. It must drive a load of 100 units. Logical effort of 4-input NAND is 6/3, logical effort of 2-input NAND is 4/3, and logical effort of inverter is 1.

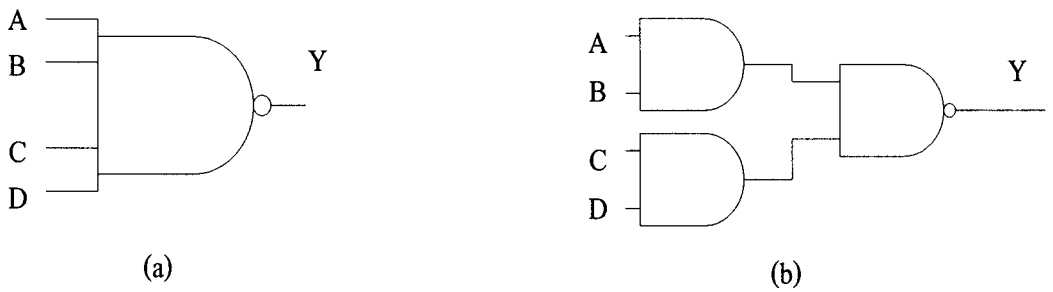


Fig. 1

a. Estimate the delay of the NAND gates in Fig 1(a) and 1(b). (10 points)

b. Estimate the area represented in the number of total transistor widths of the NAND gates in Fig 1(a) and 1(b). (10 points)

c. Discuss which NAND is better and describe the reason (10 points)

2. Design the best speed 2-input NAND gate for the signals A and B as shown in Fig 2. (10 points)

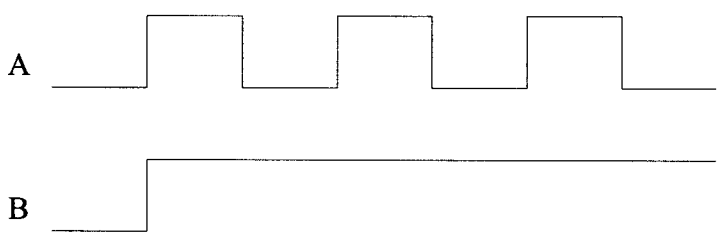


Fig. 2

3. Show and solve the charge sharing problem for the dynamic 4-input NAND gates. (10 points)

4. Assume a library has modules with delay parameters as shown in Table 1. Design a two-stage loop pipeline sequencing methods as shown in Fig 3.

Table 1

Parameter	Description	Delay (ns)
T_{pd1}	Logic 1 propagation delay	10
T_{cd1}	Logic 1 contamination delay	2
T_{pd2}	Logic 2 propagation delay	5
T_{cd2}	Logic 2 contamination delay	2
T_{pcqL}	Latch Clk-Q propagation delay	2
T_{ccqL}	Latch Clk-Q contamination delay	1
T_{pcqF}	Flop Clk-Q propagation delay	4
T_{ccqF}	Flop Clk-Q contamination delay	1
T_{pdq}	Latch D-Q propagation delay	3
T_{pcq}	Latch D-Q contamination delay	1
T_{setup}	Latch/Flop setup time	1
T_{hold}	Latch/Flop hold time	2

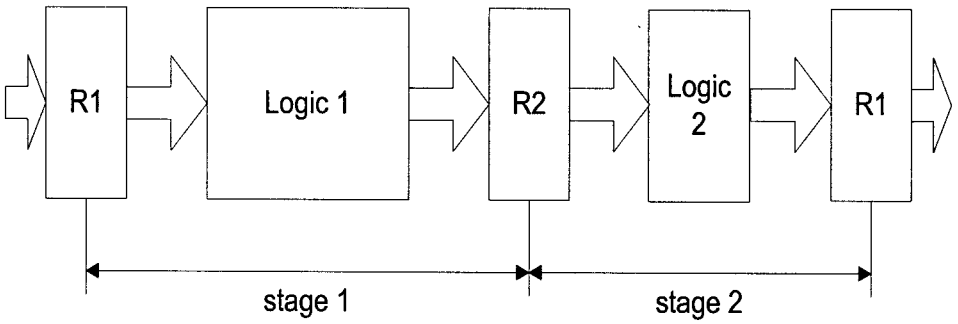


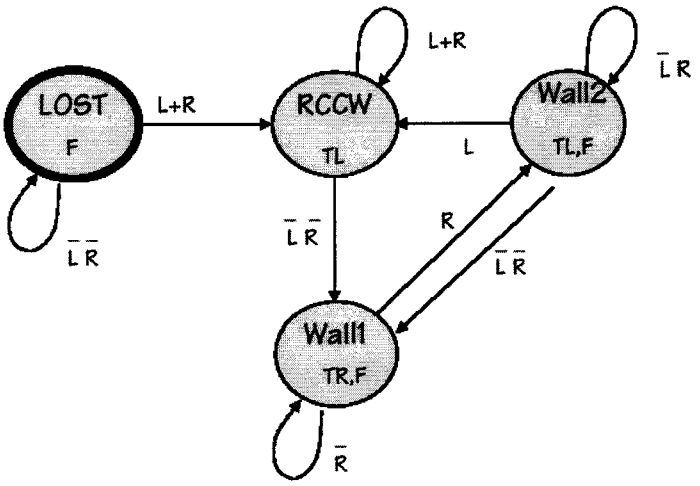
Fig. 3

a. Determine max-delay and check min-delay constraints for the flip-flop sequencing method. (10 points)

b. Apply time borrowing technique to speed up the pipeline for the 2-phase latch sequencing method. (10 points)

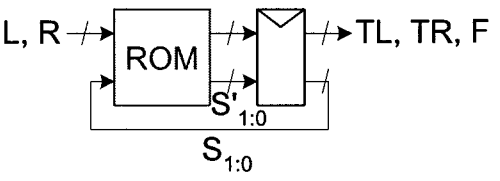
c. Discuss throughput of 4a and 4b represented in amount of data samples per second (10 points)

5. Design the following finite state machine by using ROM (20 points)



Guide: step1: Create state transition table

Present state	Inputs		Next state	Outputs		
S1:0	L	R	S1:0'	TR	TL	F
00	0	0	00	0	0	1
00	1	X	01	0	0	1
00	0	1				
01	1	X				
01	0	1				
01	0	0				
10	X	0				
10	X	1				
11	1	X				
11	0	0				
11	0	1				



Step 2: Determine sizes of ROM decoder, ROM cell, and Flip-Flops.

Step 3: Map table from step 1 to ROM cell