

Prince of Songkla University  
Engineering Faculty

Final Exam Semester 2  
Date: 1 March 2006  
240-341 Computer System Design

Academic Year: 2005  
Time: 0900-1200  
Room: R300

Instruction Notes:

- \* This examination sheet contains 6 pages, include this cover sheet
- \* There are 6 questions, attempt all questions
- \* Books and Calculator are not allowed

1. A program contains the following instruction mix
- \* 50% load/store instructions with execution of 1.2us each
  - \* 20% ALU instructions with execution time 0.8us each
  - \* 30% branch instructions with execution time of 1.0us each

1.1 if clock period is 0.2us, calculate the average CPI for the program (5 marks)

1.2 What is average MIPS rate of the program (5 marks)

2. From example programs below

```

--- MC68000 example program -----
cr      equ      13          ; define return character
len     equ      132        ; define line length

        org      $1000     ; locate line at 1000H

line    ds.b     len        ; reserve storage for len byte

        org      $2000
start   move.b   #len-1, d0  ; initialize count -1 in D0
        movea.l  #line, a0  ; starting address of array into A0
loop    cmpi.b   #cr, (a0)+ ; make compare
        dbeq    d0, loop    ; double test:
                          ; if LINE[131-D0] != 13 then decr D0
                          ; if D0 != -1 then branch to LOOP
                          ; else fall through to next instruction
here    jmp     here

```

2.1 Modify the MC68000 assembly program to copy data from "line" storage to "line2" storage which is located at address 1800H (5 marks)

2.2 Modify the MC68000 assembly program to "search and replace" all occurrence of 'cr' (0x0d) in "line" storage to 'lf' (0x0a) (5 marks)

```

--- SPARC example program -----

```

```

        .begin
        .org   4000H

start:  ld      [x], %r1
        ld      [y], %r2
        addcc  %r1, %r2, %r3
        st     %r3, [z]
        jmp    %r15+8, %r0 ! hint: == return from sub routine
        nop

x:      15          ! hint: use dc.l for MC68000
y:      9
z:      0
        .end

```

2.3 Write equivalent SPARC example program above using MC68000 assembly (5 marks)

2.4 Give the final result of %r0, %r1, %r2, %r3, z (5 marks)

Using 2-bus SRC Micro-architecture as shown in figure 1

3. Write concrete RTN for the following instruction (5 marks)

Instruction	Abstract RTN
ldr ra, c1	R[ra] <- M[rel] rel<31..0> := PC<31..0> + C1<21..0> {sign extend, 2's comp.}

4. From CPU operation Step and Control Sequence,  
4.1 fill Concrete RTN in the table below (5 marks)

Step	Concrete RTN	Control Sequence
T0		PCout, C=B, MAin
T1		PCout, INC4, PCin, Read, Wait
T2		MDout, C=B, IRin
T3		Grb, Rout, C=B, Ain
T4		Grc, Rout, ADD, Sra, Rin, End

4.2 What is the instruction in Q 4.1 (5 marks)

5. Using figure 2 and following instructions and their memory addresses to trace the flow of instructions

Address	Instruction	Comment
100:	add r4, r6, r8	; R[4] <- R[6] + R[8]
104:	ld r7, 128(r5)	; R[7] <- M[R[5]+128]
108:	brl r9, r11, 001	; PC <- R[11](=512):R[9] <- PC
112:	str r12, 32	; M[PC+32] <- R[12]
...	...	
512:	sub ...	; next instruction

When "add r4, r6, r8" is at stage 5 (IR5 = "add r4"), what are the value of IR2, IR3, IR4, PC, PC2 (5 marks)

6. Using the following table,

		Write to Register File Data Available Normal/Earliest, Stage			
Instruction Class		alu	load	ladr	brl
		6/4	6/5	6/4	6/2
read	alu	2/3	4/1	4/2	4/1
from	load	2/3	4/1	4/2	4/1
reg.	ladr	2/3	4/1	4/2	4/1
file	store(rb)	2/3	4/1	4/2	4/1
	store(ra)	2/4	4/1	4/1	4/1
	branch	2/2	4/2	4/3	4/2

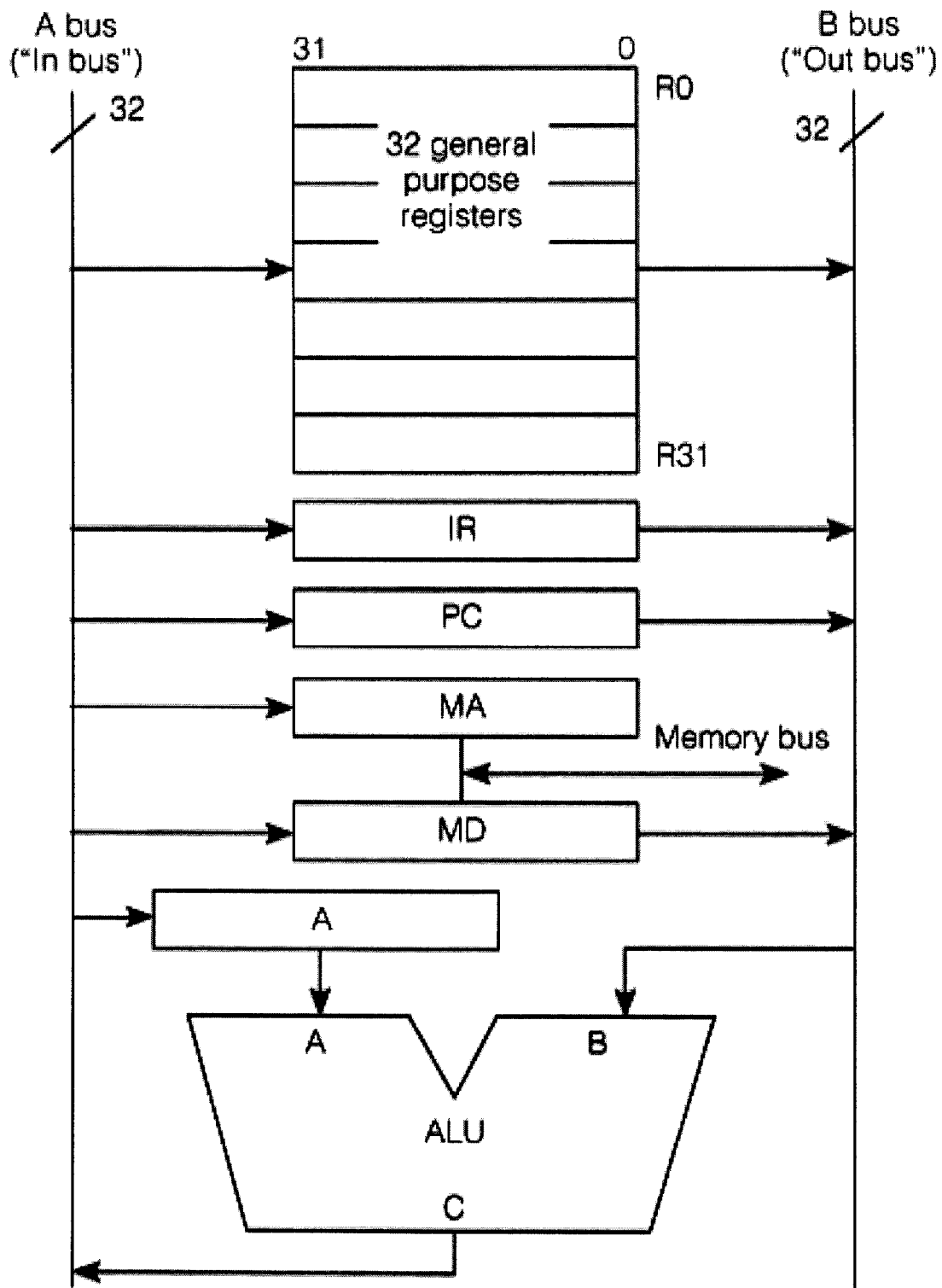
for the following pairs of SRC instructions,

- a.    ld r2, (r4)  
      add r6, r4, r2
- b.    add r0, r2, r4  
      sub r6, r0, r0
- c.    lar r31, -12  
      br r31
- d.    add r0, r2, r4  
      st r0, 12(r2)
- e.    add r0, r2, r4  
      st r2, 12(r0)

indicate how many bubbles must be placed between this pairs of instructions to resolve dependence if

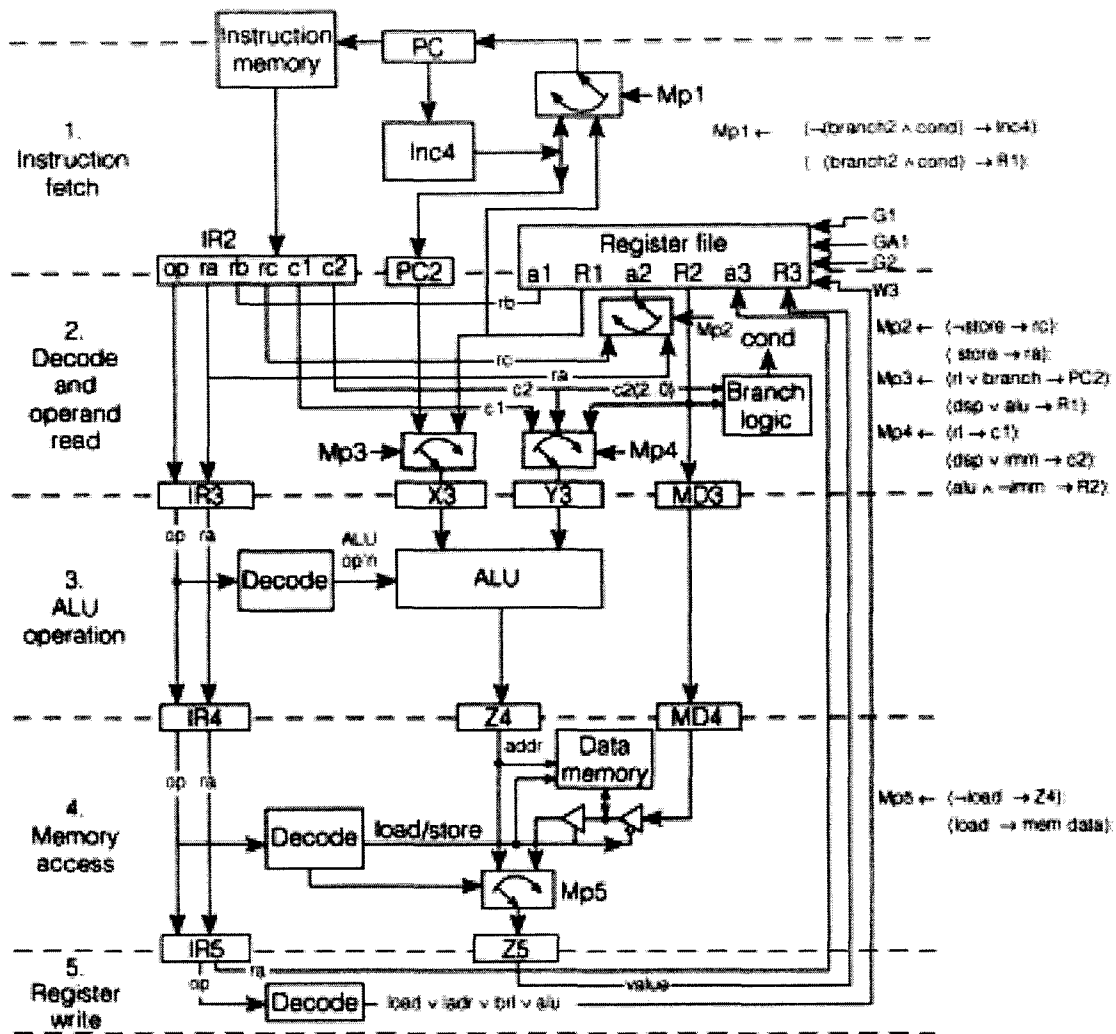
- 6.1 cpu has data forwarding (5 marks)
- 6.2 cpu doesn't has data forwarding (5 marks)

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figure 1



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figure 2