มหาวิทยาลัยสงขลานครินทร์

คณะวิศวกรรมศาสตร์

การสอบปลายภาค ประจำภาคการศึกษาที่ 2	ปีการศึกษา : 2550
วันที่ : 5 ตุลาคม พ.ศ. 2550	เวลา : 9:00 – 12:00
วิชา : 240-205 Digital Systems and Logic Design	ห้อง : หัวหุ่น
241-208 Digital Systems and Logic Design	R300

ทุจริตในการสอบ โทษขั้นต่ำคือ ปรับตกในรายวิชาที่ทุจริต และพักการเรียนหนึ่งภาคการศึกษา

<u>คำสั่ง</u>

1. ข้อสอบมีทั้งหมด 8 ข้อ 20 หน้า (ไม่รวมปก)
2. ให้แสดงวิธีทำโดยละเอียดในข้อสอบ แต่ละข้อคะแนนไม่เท่ากัน
3. ห้ามนำเครื่องคิดเลข, เอกสารใดๆ เข้าห้องสอบ
4. คำตอบทุกข้อเขียนให้ชัดเจน ถ้าอ่านไม่ออกถือว่าตอบผิด

รหัสนักศึกษา:_____ชื่อ:_____Section:_____

คำถาม	1(15)	2(4)	3(14)	4(24)	5(8)	6(10)	7(10)	8(5)	รวม(90)
คะแนน									

1. จงตอบคำถามต่อไปนี้

1.1) จงออกแบบวงจร Half Adder (4 คะแนน)

ตอบ

1.2) จงสร้างวงจร Full adder โดยใช้วงจร Half Adder (6 คะแนน)

ตอบ

1.3) จงบอกข้อเสียของการสร้างวงจรบวกเลขหลาย ๆ บิตแบบ Ripple(Asynchronous) Carry และบอกวิธีการแก้ไขข้อเสียดังกล่าว (2 คะแนน)

ตอบ _____

_____

_____

1.4) จงสร้างวงจรเพื่อเก็บค่า "1" ลงใน register เมื่อกำหนดให้สถานะเริ่มต้นมีค่าเป็น "0"

(2 คะแนน)

1.5) อินพุตแบบใดของฟลิบฟลอบที่ให้เอาต์พุตโดยไม่ขึ้นกับสัญญาณนาฬิกา (2 คะแนน)

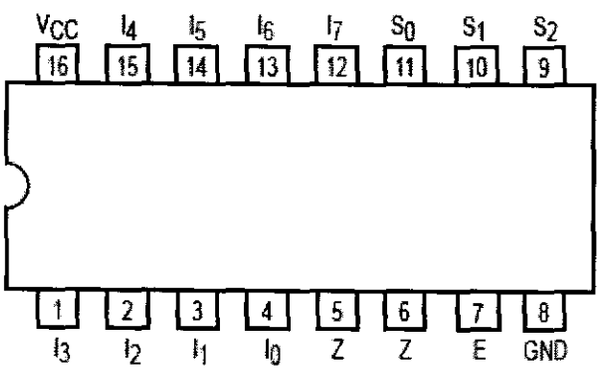
ตอบ _____

2. จงสร้างวงจรโดยใช้ Connection diagram ที่กำหนดให้ ให้มีการทำงานเหมือนในตารางค่าความจริง ตารางที่ 1 และให้ใช้ไอซี 74LS150 Line Data Selector/Multiplexer (ดูข้อมูลเพิ่มเติมใน Appendix) กับเกตพื้นฐานเท่านั้นในการสร้างวงจร (4 คะแนน)

ตารางที่ 1

C	B	A	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

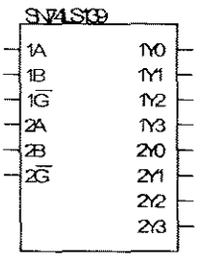
ตอบ

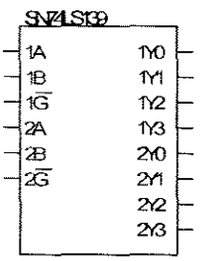


3. จากไอซี 74LS139 Decoder/Demultiplexers จงตอบคำถามต่อไปนี้

3.1) จงนำไอซี 74LS139 มาสร้างวงจร 4-to-16 Line Decoder พร้อมทั้งระบุขาอินพุต และขาเอาต์พุต O_0-O_{15} ให้ครบถ้วน (ดูข้อมูลเพิ่มเติมจาก Appendix) (9 คะแนน)

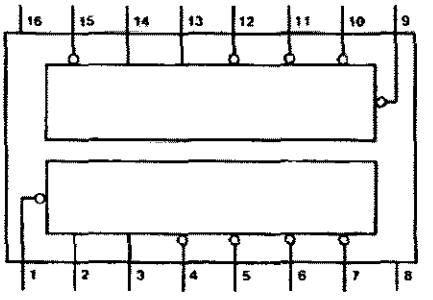
ตอบ





3.2) จาก connection diagram ที่กำหนดให้ จงออกแบบวงจร Demultiplexer โดยใช้ไอซี 74LS139 (ดูข้อมูลเพิ่มเติมจาก Appendix) (5 คะแนน)

ตอบ



4. กำหนดให้ลอจิก Y = 1 เป็นลอจิกที่ใช้ควบคุมระบบการเปิดล็อคของระบบหนึ่ง เพื่อเปิดล็อคจะต้องป้อนรหัส A และ B ให้ถูกต้อง ถ้าสมมุติให้สถานะเริ่มต้นของระบบเป็นสถานะ "closed" เมื่อป้อนรหัส 01 ระบบก็จะเปลี่ยนสถานะเป็น "1/3 Open" จากสถานะนี้ถ้าป้อนรหัส 10 ระบบก็จะเปลี่ยนสถานะเป็น "2/3 Open" และจากสถานะนี้ถ้าป้อนรหัส 11 ระบบก็จะเข้าสู่สถานะ "Open" และที่สถานะนี้ระบบจะทำการสร้างลอจิก Y = 1 เพื่อใช้เปิดล็อค จากนั้นระบบก็จะเปลี่ยนเป็นสถานะ "closed" อัตโนมัติ ในขณะที่ระบบอยู่ในสถานะต่างๆ เมื่อกดรหัสผิด ระบบจะกลับไปเป็นสถานะ "closed" เสมอ จากข้อมูลที่กำหนดให้ตอบคำถามต่อไปนี้

4.1 เขียน state diagram ของระบบดังกล่าว (2 คะแนน)

ตอบ

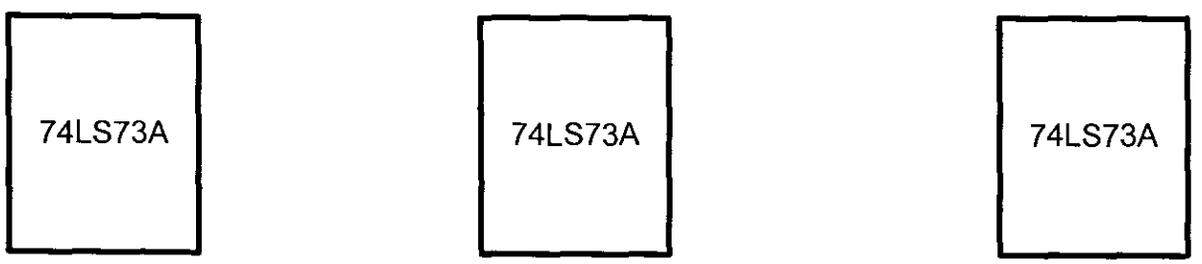
4.2 จงสร้าง state table ของระบบซึ่งประกอบด้วยอินพุต A, B, C, สถานะปัจจุบัน, ,สถานะต่อไป และเอาต์พุตทุกเอาต์พุต รวมทั้งลอจิก Z เมื่อกำหนดจำนวนบิตฐานสองที่จำเป็นสำหรับการแทนแต่ละ state ให้กับระบบในแต่ละสถานะ (8 คะแนน)

ตอบ

4.3 จงออกแบบวงจรเพื่อเปิดล็อคโดยใช้ JK flip-flop และ combination logic gate (9 คะแนน)

ตอบ

4.4 จงวาดวงจรที่ได้ในข้อ 4.3 โดยใช้ไอซี 74LS73A (ไม่ต้องระบุขา Vcc และ GND) (5 คะแนน)



5. กำหนดให้ state table ดังตารางที่ 2 จงตอบคำถามต่อไปนี้

ตารางที่ 2

Q_N			Q_{N+1}			J,K F/F					
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	1	1	1	1	1	X	1	X	X	0
1	1	1	1	0	1	X	0	X	1	X	0
1	0	1	0	1	1	X	1	1	X	X	0
0	1	1	0	0	1	0	X	X	1	X	0
0	0	0	X	X	X	X	X	X	X	X	X
0	1	0	X	X	X	X	X	X	X	X	X
1	0	0	X	X	X	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X	X	X	X

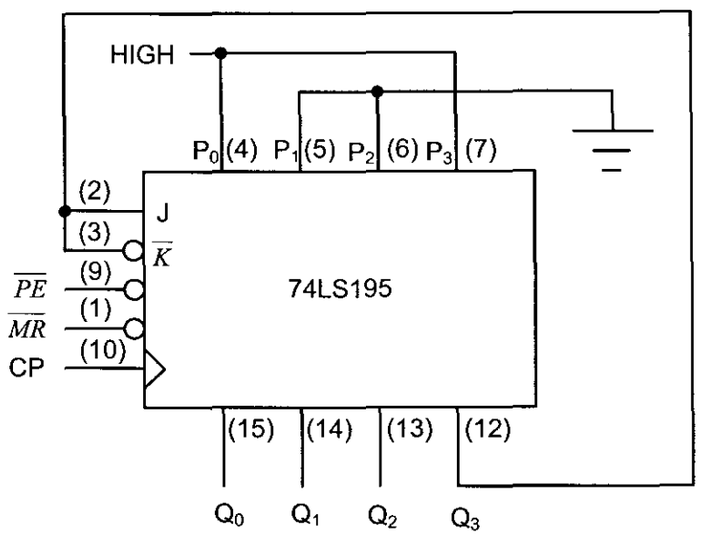
5.1) จงเขียน State Diagram ของวงจรนับ (2 คะแนน)

ตอบ

5.2) จงหาสมการลอจิกของวงจรนับ และลดรูปสมการให้เหลือน้อยที่สุด (6 คะแนน)

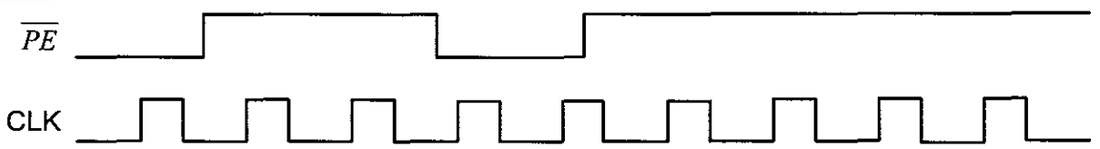
ตอบ

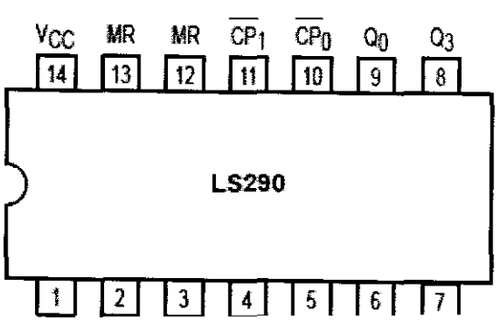
6. จงเขียน Timing Diagram ของสัญญาณ Q_0, Q_1, Q_2, Q_3 ของวงจรรูปที่ 6.1 (10 คะแนน)



รูปที่ 6.1

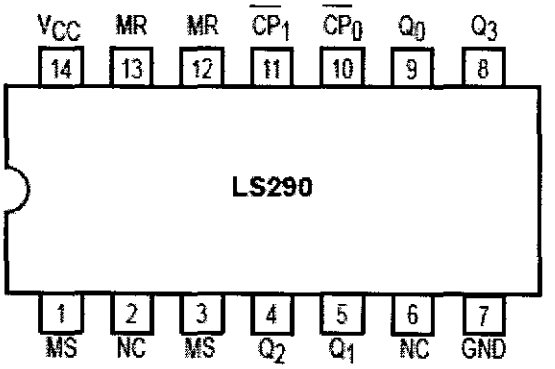
ตอบ

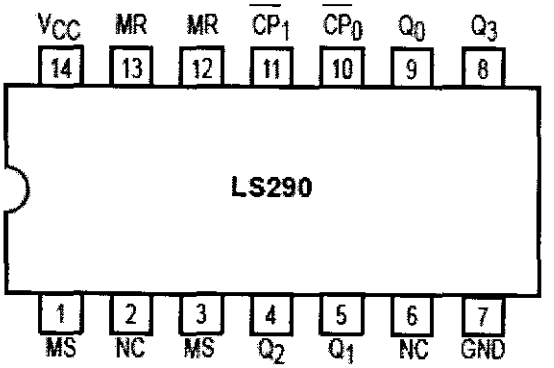




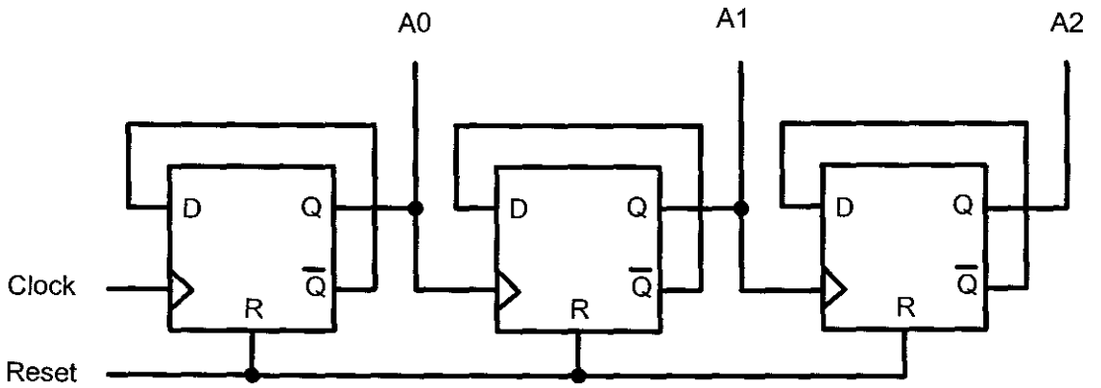
7. จงออกแบบวงจรหารความถี่ด้วย 30 โดยใช้ IC 74LS290 และให้มี duty cycle 50%
(ดูข้อมูลเพิ่มเติมได้จาก Appendix) (9 คะแนน)

ตอบ





8. จากวงจรรูปที่ 8.1 ตอบคำถามต่อไปนี้



รูปที่ 8.1

8.1) จงเขียนลำดับการนับของวงจรรูปที่ 8.1 เมื่อกำหนดให้สถานะเริ่มต้นเป็น 000 (2 คะแนน)

ตอบ _____

_____

8.2) ให้เปลี่ยนแปลงวงจรโดยใช้ J, K ฟลิปฟลอบ (3 คะแนน)

ตอบ

APPENDIX

MOTOROLA

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

SN54/74LS73A

DUAL JK NEGATIVE
EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY

The SN54LS/74LS73A offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

J SUFFIX
CERAMIC
CASE 632-08

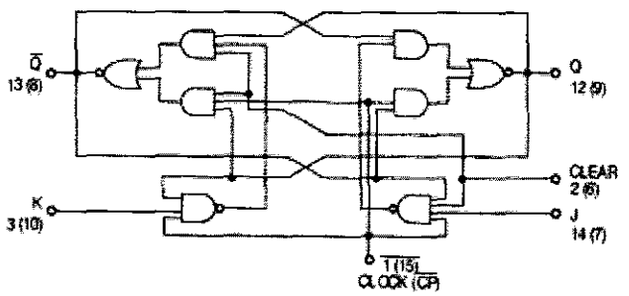
N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC DIAGRAM (Each Flip-Flop)

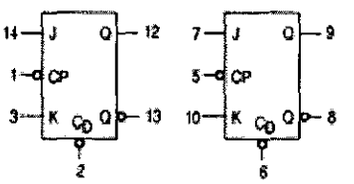


MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Reset (Clear)	L	X	X	L	H
Toggle	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	$\overline{q}$
Hold	H	l	l	q	$\overline{q}$

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition

LOGIC SYMBOL



V_{CC} = PIN 4
GND = PIN 11

National Semiconductor

June 1989

54LS138/DM54LS138/DM74LS138, 54LS139/DM54LS139/DM74LS139 Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

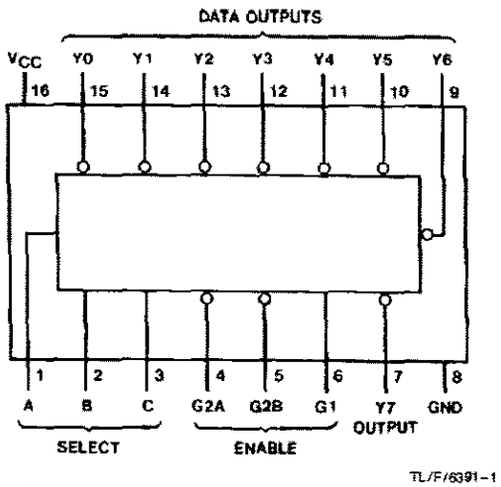
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - LS138 21 ns
  - LS139 21 ns
- Typical power dissipation
  - LS138 32 mW
  - LS139 34 mW
- Alternate Military/Aerospace devices (54LS138, 54LS139) are available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

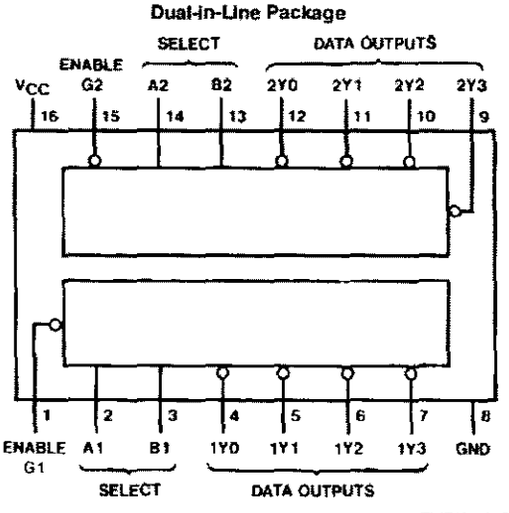
Dual-in-Line Package



TL/F/6391–1

Order Number 54LS138DMQB, 54LS138FMQB, 54LS138LMQB, DM54LS138J, DM54LS138W, DM74LS138M or DM74LS138N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Dual-in-Line Package



TL/F/6391–2

Order Number 54LS139DMQB, 54LS139FMQB, 54LS139LMQB, DM54LS139J, DM54LS139W, DM74LS139M or DM74LS139N
See NS Package Number E20A, J16A, M16A, N16E or W16A

RRD-B30M105/Printed in U. S. A.

'LS139 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.8	11	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

'LS139 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output		24		40	ns

Function Tables

LS138

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* G2 = G2A + G2B

H = High Level, L = Low Level, X = Don't Care

LS139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care

FAIRCHILD SEMICONDUCTOR™

September 1986
Revised June 2001

DM74150
Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The DM74150 selects one-of-sixteen data sources. The DM74150 has a strobe input which must be at a LOW logic level to enable these devices. A HIGH level at the strobe forces the W output HIGH and the Y output (as applicable) LOW.

The DM74150 features an inverted (W) output only.

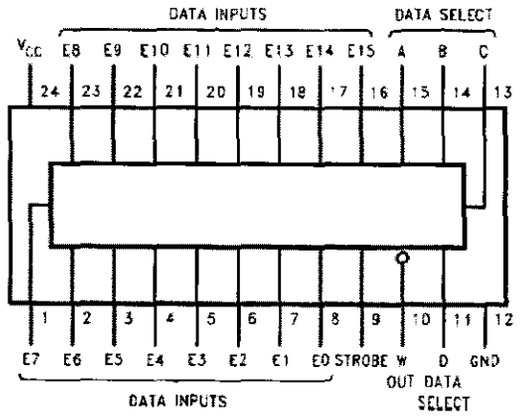
Features

- 150 selects one-of-sixteen data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time, data input to W output: 11 ns
- Typical power dissipation: 200 mW

Ordering Code:

Order Number	Package Number	Package Description
DM74150N	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600" Wide

Connection Diagram



Function Table

Inputs					Outputs
Select				Strobe	W
D	C	B	A	S	
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

H = HIGH Level
L = LOW Level
X = Don't Care
$\overline{E0}$, $\overline{E1}$ ... $\overline{E15}$ = the complement of the level of the respective E input

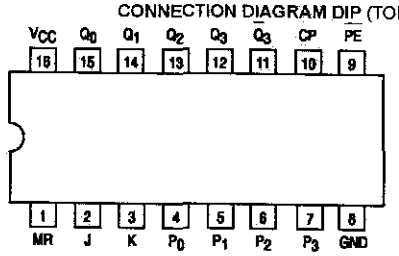
MOTOROLA

UNIVERSAL 4-BIT SHIFT REGISTER

The SN54/74LS195A is a high speed 4-Bit Shift Register offering typical shift frequencies of 39 MHz. It is useful for a wide variety of register and counting applications. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

- Typical Shift Right Frequency of 39 MHz
- Asynchronous Master Reset
- J, K Inputs to First Stage
- Fully Synchronous Serial or Parallel Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{J}$	First Stage J (Active HIGH) Input	0.5 U.L.	0.25 U.L.
K	First Stage K (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5 (2.5) U.L.
Q_3	Complementary Last Stage Output (Note b)	10 U.L.	5 (2.5) U.L.

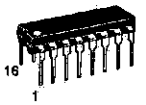
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS195A

UNIVERSAL 4-BIT SHIFT REGISTER

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 620-09



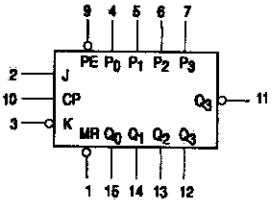
N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

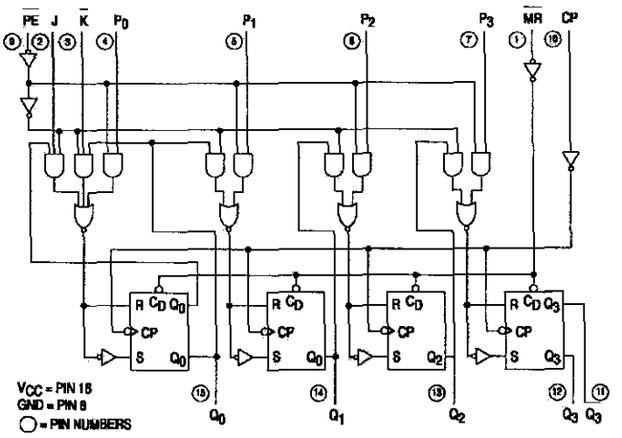
LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS195A

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS195A 4-Bit Shift Register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The LS195A has two primary modes of operation, shift right (Q_0 Q_1) and parallel load which are controlled by the state of the Parallel Enable (PE) input. When the PE input is HIGH, serial data enters the first flip-flop Q_0 via the J and K inputs and is shifted one bit in the direction Q_0 Q_1 Q_2 Q_3 following each LOW to HIGH clock transition. The JK inputs provide the flexibility of the JK type input for special applications, and the simple D type input for general applications by tying the two pins together. When the $\overline{PE}$ input is LOW, the LS195A appears as four common clocked D flip-flops. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs following the LOW to HIGH clock transition. Shift left operations (Q_3 Q_2) can be achieved by tying the Q_n Outputs to the P_{n-1} inputs and holding the PE input LOW.

All serial and parallel data transfers are synchronous, occurring after each LOW to HIGH clock transition. Since the LS195A utilizes edge-triggering, there is no restriction on the activity of the J, K, P_n and PE inputs for logic operation — except for the set-up and release time requirements.

A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

MODE SELECT — TRUTH TABLE

OPERATING MODES	INPUTS					OUTPUTS				
	MR	PE	J	K	P_n	Q_0	Q_1	Q_2	Q_3	Q_3
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	$\overline{q_2}$
Shift, Reset First	H	h	l	l	X	L	q_0	q_1	q_2	$\overline{q_2}$
Shift, Toggle First Stage	H	h	h	l	X	q_0	q_0	q_1	q_2	$\overline{q_2}$
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	q_2
Parallel Load	H	l	X	X	p_n	p_0	p_1	p_2	p_3	$\overline{p_3}$

L = LOW voltage levels
H = HIGH voltage levels
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition.
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
c) The Q_0 Outputs are guaranteed to drive the full fan-out plus the CP_1 input of the device.

MOTOROLA

SN54/74LS290
SN54/74LS293

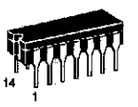
DECADE COUNTER;
4-BIT BINARY COUNTER

The SN54/74LS290 and SN54/74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS290) or divide-by-eight (LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to CP)to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the LS290 also has a 2-input gated Master Set (Preset 9).

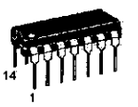
- Corner Power Pin Versions of the LS90 and LS93
- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Binary
- Input Clamp Diodes Limit High Speed Termination Effects

DECADE COUNTER;
4-BIT BINARY COUNTER

LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



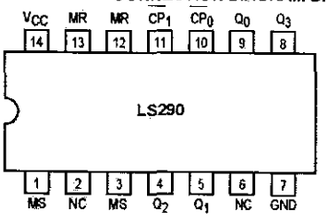
N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

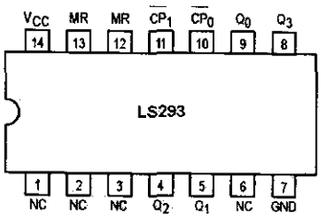
ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



PIN NAMES

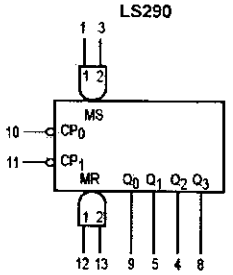
		LOADING (Note a) HIGH	LOW
$\overline{CP_0}$	Clock (Active LOW going edge) Input to ÷2 Section.	0.05 U.L.	1.5 U.L.
$\overline{CP1}$	Clock (Active LOW going edge) Input to ÷5 Section (LS290).	0.05 U.L.	2.0 U.L.
CP1	Clock (Active LOW going edge) Input to ÷8 Section (LS293).	0.05 U.L.	1.0 U.L.
MR1, MR2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS1, MS2	Master Set (Preset-9, LS290) Inputs	0.5 U.L.	0.25 U.L.
Q0	Output from ÷2 Section (Notes b & c)	10 U.L.	5 (2.5) U.L.
Q1, Q2, Q3	Outputs from ÷5 & ÷8 Sections (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
c) The Q_0 Outputs are guaranteed to drive the full fan-out plus the CP_1 input of the device.

SN54/74LS290 • SN54/74LS293

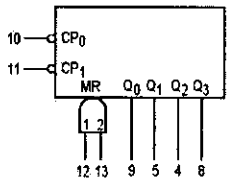
LOGIC SYMBOL

LS290



V_{CC} = PIN 14
GND = PIN 7
NC = PINS 2, 6

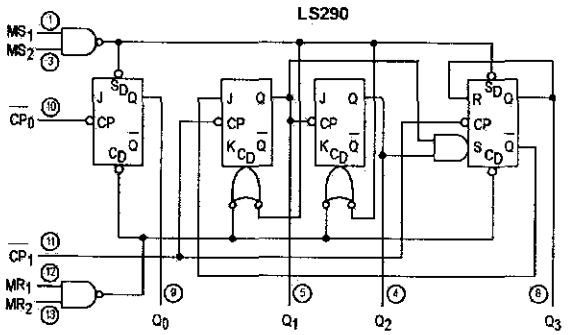
LS293



V_{CC} = PIN 14
GND = PIN 7
NC = PINS 1, 2, 3, 6

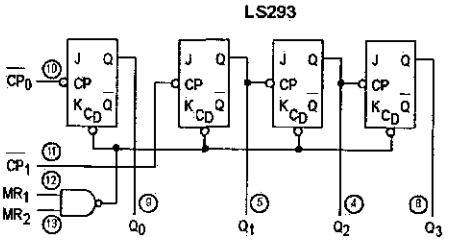
LOGIC DIAGRAMS

LS290



V_{CC} = PIN 14
GND = PIN 7
○ = PIN NUMBERS

LS293



V_{CC} = PIN 14
GND = PIN 7
○ = PIN NUMBERS

SN54/74LS290 • SN54/74LS293

FUNCTIONAL DESCRIPTION

The LS290 and LS293 are 4-bit ripple type Decade, and 4-Bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS290) or divide-by-eight (LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the CP_1 input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

LS290

A. BCD Decade (8421) Counter — the $\overline{CP_1}$ input must be externally connected to the Q_0 output. The $\overline{CP_0}$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the CP_0 input. The input count is then applied to the CP_1 input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (CP_0 as the input and Q_0 as the output). The CP_1 input is used to obtain binary divide-by-five operation at the Q_3 output.

LS293

A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input CP_1. The input count pulses are applied to input CP_0. Simultaneous division of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter — The input count pulses are applied to input CP_1. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS290 MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

LS290
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to input CP_1 for BCD count.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS293 MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input CP_1.