หมายเลขโต๊ะที่นั่งสอบ..... .

มหาวิทยาลัยสงขลานครินทร์

คณะวิศวกรรมศาสตร์

การสอบปลายภาค ประจำภาคการศึกษาที่ 2 ปีการศึกษา : 2550

วันที่ : 18 กุมภาพันธ์ พ.ศ. 2551 เวลา : 13.30 – 16.30 น

วิชา : 240-205 Digital Systems and Logic Design ห้อง : หัวหุ่น (หาดใหญ่)

241-208 Digital Systems and Logic Design 5301, 5401 (ภูเก็ต)

อาจารย์ผู้สอน : อ.ทศพร กมลภิวงศ์, อ.พัชรี เทพนิมิตร

ทุจริตในการสอบ โทษขั้นต่ำคือ ปรับตกในรายวิชาที่ทุจริต และพักการเรียนหนึ่งภาคการศึกษา

<u>คำสั่ง</u>

1. ข้อสอบมีทั้งหมด 8 ข้อ 21 หน้า (ไม่รวมปก) คะแนนรวม 80 คะแนน
2. ให้แสดงวิธีทำโดยละเอียดในข้อสอบ แต่ละข้อคะแนนไม่เท่ากัน
3. ห้ามนำเครื่องคิดเลข, เอกสารใดๆ เข้าห้องสอบ
4. คำตอบทุกข้อเขียนให้ชัดเจน ถ้าอ่านไม่ออกถือว่าตอบผิด

รหัสนักศึกษา:_____ชื่อ:_____Section:_____

คำถาม	1(6)	2(5)	3(5)	4(7)	5(7)	6(12)	7(12)	8(26)	รวม(80)
คะแนน									

1. จงตอบคำถามต่อไปนี้ (6 คะแนน)

1.1) จงบอกข้อแตกต่างระหว่างวงจร Asynchronous Counter กับวงจร Synchronous Counter ,น แง่ของการเชื่อมต่อ clock และ Propagation delay ของวงจรนับ (2 คะแนน)

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1.2) Full adder แตกต่างจาก Half Adder อย่างไร (1 คะแนน)

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1.3) จงสร้าง D ฟลิบฟลอบโดยใช้ J-K ฟลิบฟลอบ (2 คะแนน)

ตอบ

1.4) อินพุตแบบใดของฟลิบฟลอบที่ให้เอาต์พุตโดยไม่ขึ้นกับสัญญาณนาฬิกา (1 คะแนน)

ตอบ _____

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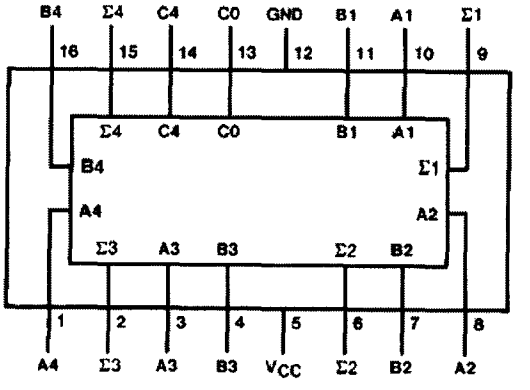
2. จงเขียน State Diagram ของวงจรนับต่อไปนี้ กำหนดให้ สถานะเริ่มต้นของการนับ คือ 0011 (5 คะแนน)

2.1) วงจรนับจอห์นสัน (Johnson counter) (3 คะแนน)

2.2) วงจรนับวงแหวน (Ring counter) (2 คะแนน)

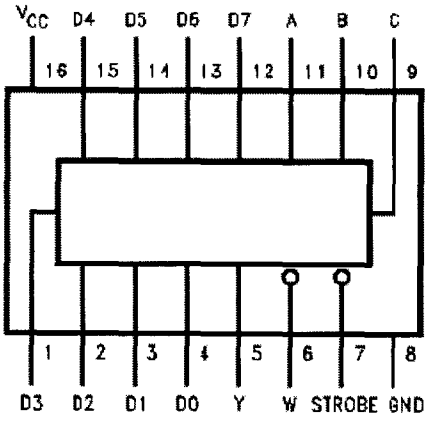
3. จงออกแบบวงจรลบเลข 4 บิต ($A_3A_2A_1A_0$ - $B_3B_2B_1B_0$) โดยใช้ไอซี DM74LS83A 4-Bit Binary Adder with Fast Carry และลอจิกเกตพื้นฐานตามความเหมาะสม พร้อมทั้งระบุขาอินพุต, ขาเอาท์พุต ($O_3O_2O_1O_0$) และขาอื่น ๆ มาให้ครบถ้วน (ดูข้อมูลไอซีเพิ่มเติมจาก Appendix) (5 คะแนน)

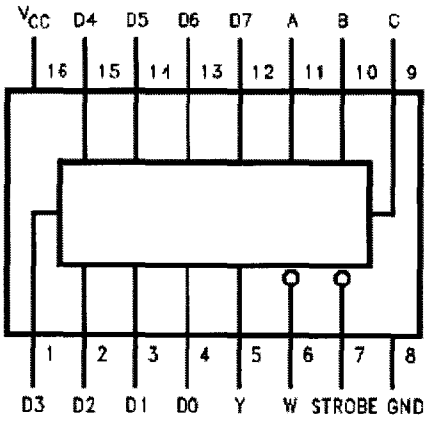


4. จงออกแบบวงจรโดยใช้ไอซี DM74151A Data Selectors/Multiplexers ให้มีค่าผลลัพธ์ดังตารางความจริงที่กำหนดให้ เมื่อ I_0, I_1, I_2, I_3 เป็นสัญญาณอินพุต และ Out เป็นสัญญาณเอาท์พุต (ดูข้อมูลไอซีเพิ่มเติมจาก Appendix) (7 คะแนน)

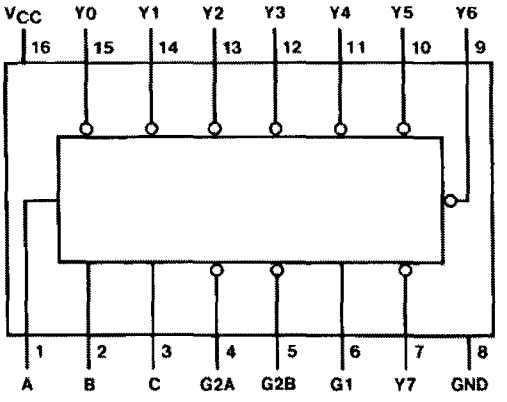
I_3	I_2	I_1	I_0	Out
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0

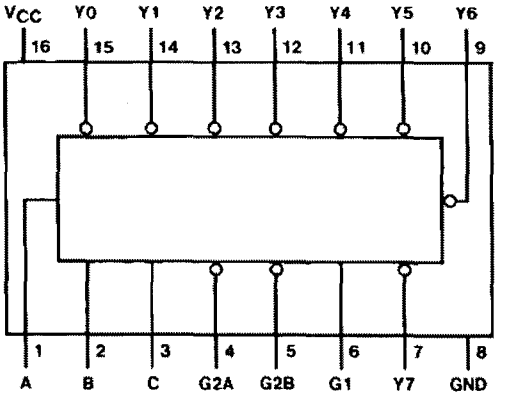
I_3	I_2	I_1	I_0	Out
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0



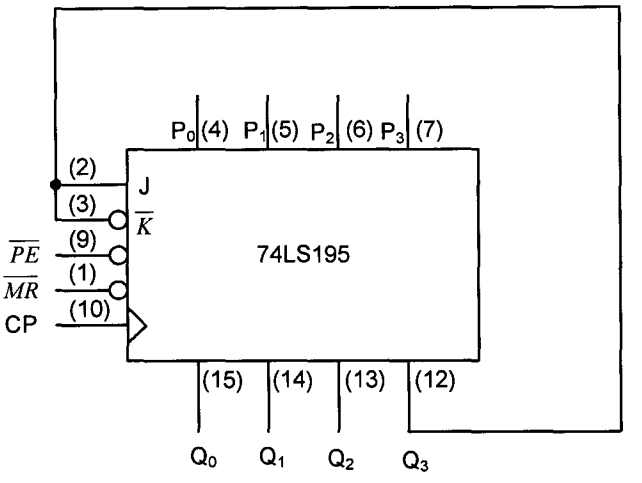


5. จากไอซี DM74LS138 3-to-8 Line Decoder/Demultiplexer จงนำมาสร้างเป็นวงจร 1 Line -to- 6 Line Demultiplexer พร้อมทั้งระบุขาอินพุตข้อมูล (I), ขาอินพุตตัวเลือก ($S_3S_2S_1S_0$) และขาเอาต์พุต (O_0-O_{15}) ให้ครบถ้วน (ดูข้อมูลไอซีเพิ่มเติมจาก Appendix) (7 คะแนน)

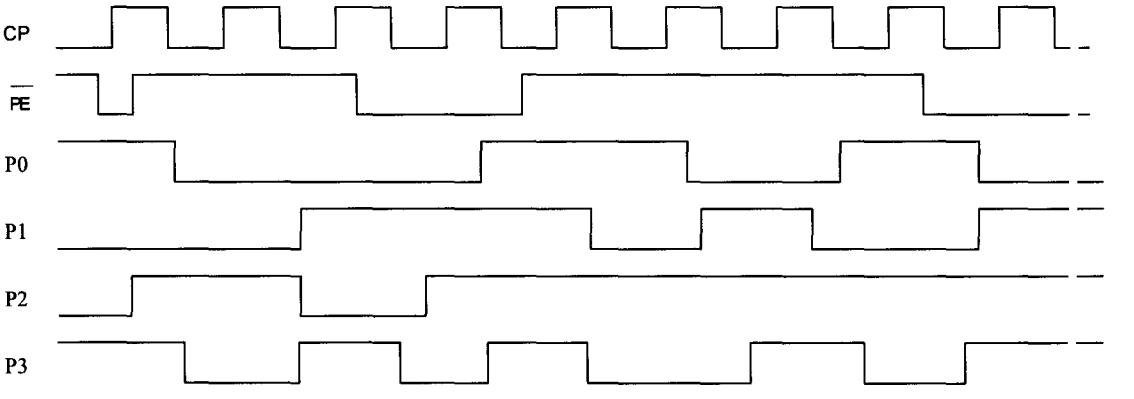




6. จากวงจรดังรูปที่ 6.1 จงเขียน Timing Diagram ของเอาท์พุต เมื่อกำหนดค่าอินพุตต่าง ๆ มาให้ดังรูป กำหนดให้ ไอซีมีสถานะเริ่มต้นเป็น Reset และสัญญาณ $\overline{MR}$ เป็น High (12 คะแนน)



รูปที่ 6.1



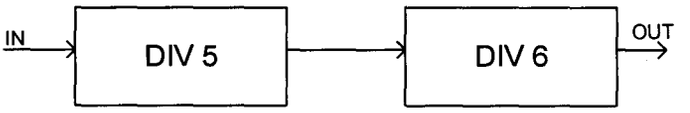
Q0

Q1

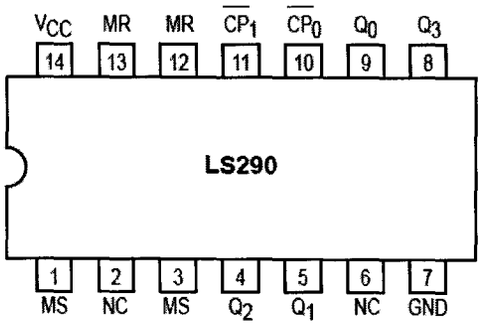
Q2

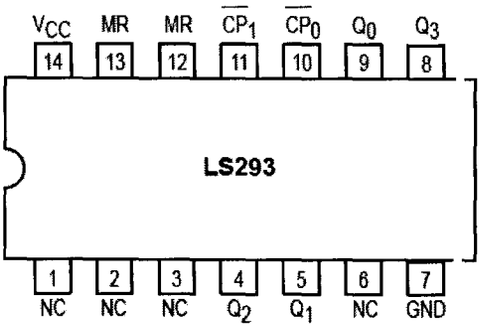
Q3

7. จากบล็อกไดอะแกรมดังรูป บล็อกแรกเป็นวงจรหารความถี่ 5 ส่วนบล็อกที่สองเป็นวงจรหารความถี่ ๖ จงตอบคำถามต่อไปนี้ (12 คะแนน)



7.1) จงออกแบบวงจรหารความถี่ตามบล็อกที่กำหนดให้ โดยใช้ IC 74LS290 และ 74LS293 (ดูข้อมูลไอซีเพิ่มเติมได้จาก Appendix) (5 คะแนน)





7.2) จากวงจรที่ออกแบบในข้อ 7.1 ถ้าป้อนสัญญาณอินพุตความถี่ 180 kHz สัญญาณที่วัดได้ที่เอาท์พุตจะมีค่าความถี่และค่า Duty Cycle เท่ากับเท่าไร (2 คะแนน)

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7.3) ถ้าต้องการแก้ไขวงจรให้มีค่า Duty Cycle 50% ควรแก้ไขวงจรที่ออกแบบในข้อ 7.1 อย่างไร พร้อมทั้งวาดวงจรที่ทำการออกแบบใหม่ (5 คะแนน)

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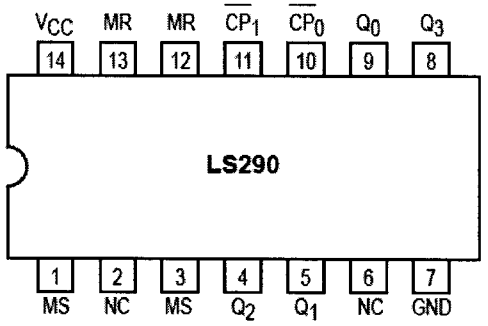
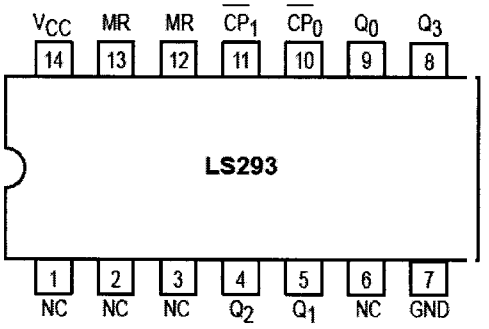




8. วงจรสำหรับการควบคุมระบบเปิดล็อคมีอินพุต 3 อินพุต คือ W, X และ Y และหนึ่งเอาต์พุต คือ Z การล็อคของระบบจะถูกเปิดเมื่อป้อนรหัสฐานสองผ่านทางอินพุต W, X และ Y สำหรับการทำงานของระบบเป็นดังนี้

เริ่มต้นระบบด้วยสถานะ "closed" เมื่อป้อนรหัส WXY = 001 ทำให้ระบบเปลี่ยนไปเป็นสถานะ "1/3-Open" และจากสถานะนี้ ถ้าป้อนรหัส WXY = 101 ระบบก็จะเปลี่ยนสถานะเป็น "2/3-Open" และจากสถานะ 2/3-Open เมื่อป้อนรหัส WXY = 011 ระบบก็จะเปลี่ยนเป็นสถานะ Open ซึ่งมีผลทำให้ระบบล็อคถูกเปิด หลังจากนั้นระบบก็จะเปลี่ยนเป็นสถานะ Closed โดยอัตโนมัติ สำหรับการป้อนรหัสที่สถานะใด ๆ ผิดพลาด จะมีผลทำให้ระบบกลับไปที่สถานะ Closed เสมอ กำหนดให้ลอจิก Z = 1 ใช้สำหรับการเปิดล็อค

จากข้อมูลที่กำหนดให้ จงตอบคำถามต่อไปนี้ (26 คะแนน)

8.1) จงเขียน state diagram ของระบบดังกล่าว (3 คะแนน)

8.2) จงกำหนดลำดับการนับเพื่อแทนสถานะต่าง ๆ ของระบบดังกล่าว (2 คะแนน)

8.3) จงสร้าง state table ของระบบ ซึ่งประกอบด้วยรหัส W, X, Y, สถานะปัจจุบัน, สถานะต่อไป และ เอาต์พุต Z (9 คะแนน)

8.4) จงออกแบบวงจรเพื่อเปิดล็อคโดยใช้ JK flip-flop และ combination logic gate (12 คะแนน)

APPENDIX

National Semiconductor

May 1989

54LS83A/DM54LS83A/DM74LS83A
4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

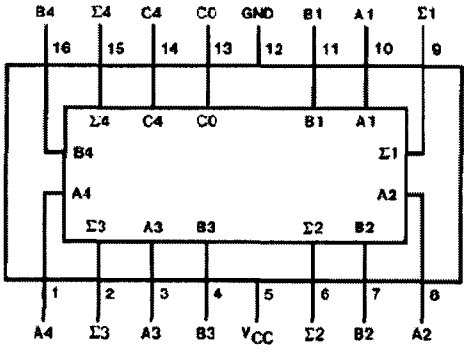
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  - Two 8-bit words 25 ns
  - Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW
- Alternate Military/Aerospace device (54LS83A) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6378–1

Order Number 54LS83ADMQB, 54LS83AFMQB,
DM54LS83AJ, DM54LS83AW, DM74LS83AWM or DM74LS83AN
See NS Package Number J16A, M16B, N16E or W16A

54LS83A/DM54LS83A/DM74LS83A 4-Bit Binary Adders with Fast Carry

FAIRCHILD SEMICONDUCTOR TM

March 1998

DM74150, DM74151A Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The 150 selects one-of-sixteen data sources; the 151A selects one-of-eight data sources. The 150 and 151A have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high and the Y output (as applicable) low.

The 151A features complementary W and Y outputs, whereas the 150 has an inverted (W) output only.

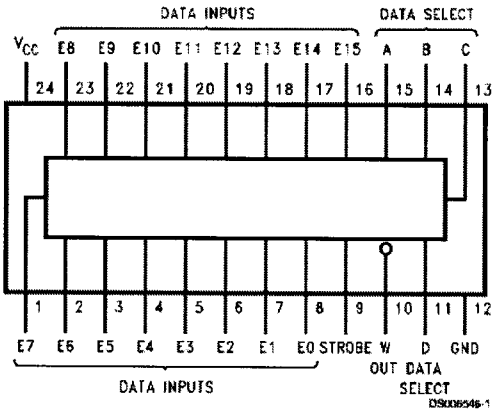
The 151A incorporates address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the 151A outputs are enabled (i.e., strobe low).

Features

- 150 selects one-of-sixteen data lines
- 151A selects one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time, data input to W output
  - 150 11 ns
  - 151A 9 ns
- Typical power dissipation
  - 150 200 mW
  - 151A 135 mW
- Alternate Military/Aerospace device (54150, 54151A) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

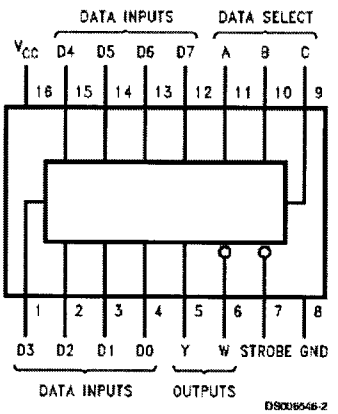
Connection Diagrams

Dual-In-Line Package



Order Number 54150DQMB, 54150FMQB, DM54150J or DM74150N
See Package Number J24A, N24A or W24C

Dual-In-Line Package



Order Number 54151ADMQB, 54151AFMQB, DM54151AJ, DM54151AW or DM74151AN
See Package Number J16A, N16E or W16A

Function Tables

54150/74150

Inputs					Outputs
Select				Strobe	W
D	C	B	A	S	
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

H = High Level, L = Low Level, X = Don't Care
$\overline{E0}$, $\overline{E1}$ ...$\overline{E15}$ = the complement of the level of the respective E input

54151A/75151A

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care
D0, D1...D7 = the level of the respective D input

National Semiconductor

June 1989

54LS138/DM54LS138/DM74LS138, 54LS139/DM54LS139/DM74LS139 Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

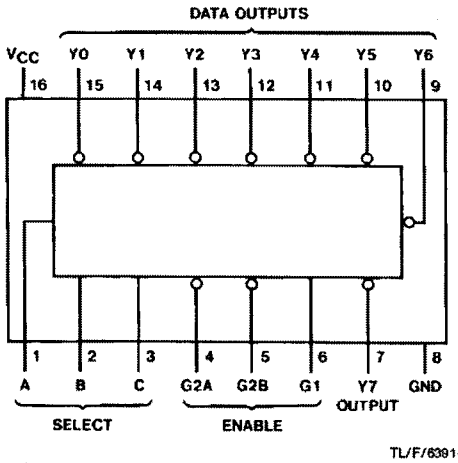
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - LS138 21 ns
  - LS139 21 ns
- Typical power dissipation
  - LS138 32 mW
  - LS139 34 mW
- Alternate Military/Aerospace devices (54LS138, 54LS139) are available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

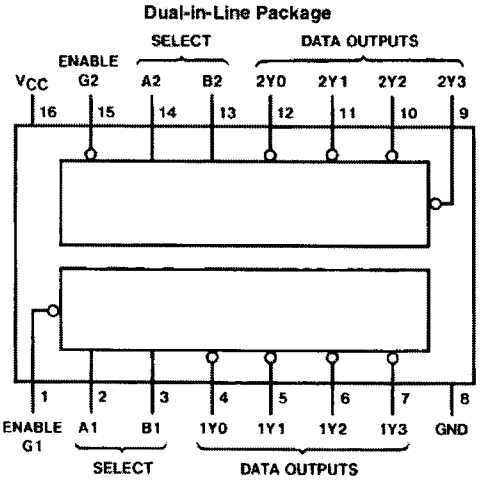
Dual-in-Line Package



TL/F/6391–1

Order Number 54LS138DMQB, 54LS138FMQB, 54LS138LMQB, DM54LS138J, DM54LS138W, DM74LS138M or DM74LS138N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Dual-in-Line Package



TL/F/6391–2

Order Number 54LS139DMQB, 54LS139FMQB, 54LS139LMQB, DM54LS139J, DM54LS139W, DM74LS139M or DM74LS139N
See NS Package Number E20A, J16A, M16A, N16E or W16A

RRD-B30M105/Printed in U. S. A.

'LS139 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.8	11	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

'LS139 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output		24		40	ns

Function Tables

LS138

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* G2 = G2A + G2B

H = High Level, L = Low Level, X = Don't Care

LS139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care

MOTOROLA

SN54/74LS195A

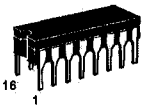
UNIVERSAL 4-BIT SHIFT REGISTER

The SN54/74LS195A is a high speed 4-Bit Shift Register offering typical shift frequencies of 39 MHz. It is useful for a wide variety of register and counting applications. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

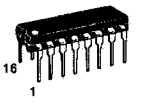
- Typical Shift Right Frequency of 39 MHz
- Asynchronous Master Reset
- J, K Inputs to First Stage
- Fully Synchronous Serial or Parallel Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects

UNIVERSAL 4-BIT SHIFT REGISTER

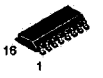
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

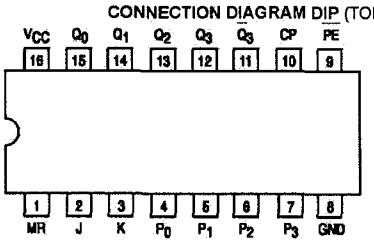


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)

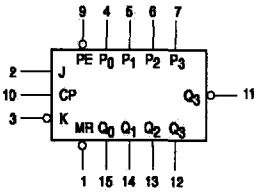


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
J	First Stage J (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{K}$	First Stage K (Active LOW) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Q_3}$	Complementary Last Stage Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

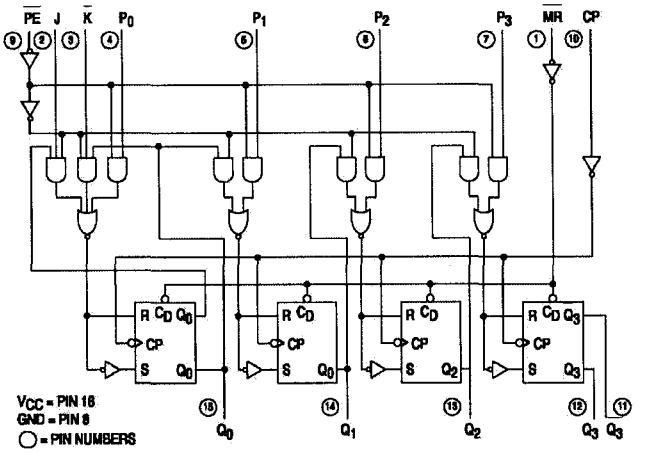
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS195A

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS195A 4-Bit Shift Register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The LS195A has two primary modes of operation, shift right (Q_0 Q_1) and parallel load which are controlled by the state of the Parallel Enable (PE) input. When the PE input is HIGH, serial data enters the first flip-flop Q_0 via the J and K inputs and is shifted one bit in the direction Q_0 Q_1 Q_2 Q_3 following each LOW to HIGH clock transition. The JK inputs provide the flexibility of the JK type input for special applications, and the simple D type input for general applications by tying the two pins together. When the $\overline{PE}$ input is LOW, the LS195A appears as four common clocked D flip-flops. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs following the LOW to HIGH clock transition. Shift left operations (Q_3 Q_2) can be achieved by tying the Q_n Outputs to the P_{n-1} inputs and holding the PE input LOW.

All serial and parallel data transfers are synchronous, occurring after each LOW to HIGH clock transition. Since the LS195A utilizes edge-triggering, there is no restriction on the activity of the J, K, P_n and $\overline{PE}$ inputs for logic operation — except for the set-up and release time requirements.

A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

MODE SELECT — TRUTH TABLE

OPERATING MODES	INPUTS					OUTPUTS				
	$\overline{MR}$	$\overline{PE}$	J	$\overline{K}$	P_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q_3}$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	$\overline{q_2}$
Shift, Reset First	H	h	l	l	X	L	q_0	q_1	q_2	$\overline{q_2}$
Shift, Toggle First Stage	H	h	h	l	X	q_0	q_0	q_1	q_2	$\overline{q_2}$
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q_2}$
Parallel Load	H	l	X	X	p_n	p_0	p_1	p_2	p_3	$\overline{p_3}$

L = LOW voltage levels
H = HIGH voltage levels
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition.
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

MOTOROLA

SN54/74LS290
SN54/74LS293

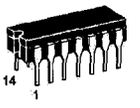
DECADE COUNTER;
4-BIT BINARY COUNTER

The SN54/74LS290 and SN54/74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS290) or divide-by-eight (LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to CP)to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the LS290 also has a 2-input gated Master Set (Preset 9).

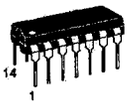
- Corner Power Pin Versions of the LS90 and LS93
- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Binary
- Input Clamp Diodes Limit High Speed Termination Effects

DECADE COUNTER;
4-BIT BINARY COUNTER

LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



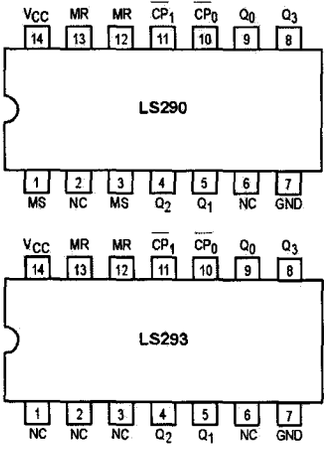
N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

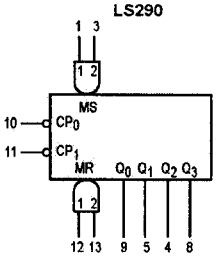
		LOADING (Note a) HIGH	LOW
$\overline{CP_0}$	Clock (Active LOW going edge) Input to ÷2 Section.	0.05 U.L.	1.5 U.L.
$\overline{CP1}$	Clock (Active LOW going edge) Input to ÷5 Section (LS290).	0.05 U.L.	2.0 U.L.
CP1	Clock (Active LOW going edge) Input to ÷8 Section (LS293).	0.05 U.L.	1.0 U.L.
MR1, MR2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS1, MS2	Master Set (Preset-9, LS290) Inputs	0.5 U.L.	0.25 U.L.
Q0	Output from ÷2 Section (Notes b & c)	10 U.L.	5 (2.5) U.L.
Q1, Q2, Q3	Outputs from ÷5 & ÷8 Sections (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
c) The Q_0 Outputs are guaranteed to drive the full fan-out plus the CP_1 input of the device.

SN54/74LS290 • SN54/74LS293

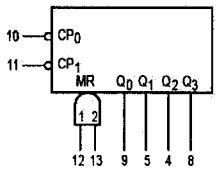
LOGIC SYMBOL

LS290



V_{CC} = PIN 14
GND = PIN 7
NC = PINS 2, 6

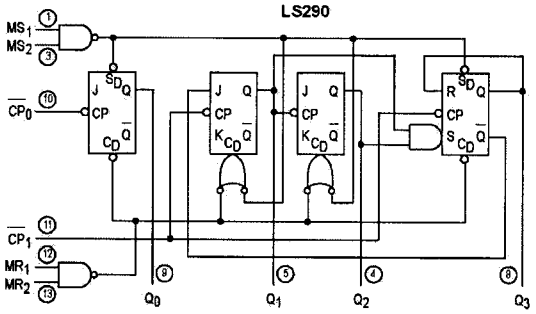
LS293



V_{CC} = PIN 14
GND = PIN 7
NC = PINS 1, 2, 3, 6

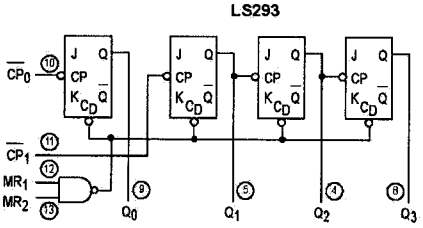
LOGIC DIAGRAMS

LS290



V_{CC} = PIN 14
GND = PIN 7
○ = PIN NUMBERS

LS293



V_{CC} = PIN 14
GND = PIN 7
○ = PIN NUMBERS

SN54/74LS290 • SN54/74LS293

FUNCTIONAL DESCRIPTION

The LS290 and LS293 are 4-bit ripple type Decade, and 4-Bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS290) or divide-by-eight (LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

LS290

A. BCD Decade (8421) Counter — the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the CP_0 input. The input count is then applied to the CP_1 input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (CP_0 as the input and Q_0 as the output). The CP_1 input is used to obtain binary divide-by-five operation at the Q_3 output.

LS293

A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input CP_1. The input count pulses are applied to input CP_0. Simultaneous division of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter — The input count pulses are applied to input CP_1. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS290 MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

LS290
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to input CP_1 for BCD count.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS293 MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input CP_1.