Name: _____ Student ID: _____

PRINCE OF SONGKLA UNIVERSITY

FACULTY OF ENGINEERING

Final Examination: Semester 1 **Academic Year**: 2011

Date: October 9th, 2011 **Time**: 13.30-16.30

Subject Number: 241-307 **Room**: หัวหุ่นยนต์, A100, R201

Subject Title: Computer Systems Architecture and Organization

Lecturer: Dr. Panyayot Chaikan and Dr. Jerry LeMieux

Exam Duration: 3 hours

This exam has 16 pages.

Authorized Materials:

- Writing instruments (e.g. pens, pencils).
- Books (e.g. dictionaries, textbooks) notes and calculators are **not** permitted.

Instructions to Students:

- *Answer questions in English.* Perfect English is **not** required.
- Attempt all questions.
- Write your answers in the space provided.
- Clearly number your answers.
- Any unreadable parts will be considered wrong.
- When writing programs, use good layout, and short comments; marks will not be deducted for minor syntax errors.
- The points for each question are given in brackets (…).

Cheating in this examination:

Lowest punishment: Failed in this subject and courses dropped for next semester.
Highest punishment: Expelled.

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Part 1: True or False **(10 points)**

1. T/F – A less complex instruction representation also calls for a simpler processor.
2. T/F – Arithmetic shifts can change the sign of the input number.
3. T/F – Operand data can be represented in any order in an instruction.
4. T/F – Addressing modes define whether operand values are reside in registers or in memory.
5. T/F – Instruction lengths can be of any arbitrary size.
6. T/F – A WAW hazard occurs only if two consecutive instructions want to write to the same memory location.
7. T/F – More than one pipeline can be implemented in a system.
8. T/F – RISC architecture has a very simple instruction set.
9. T/F – CISC's reduction in the number of instructions for a program, shows a drastic improvement in execution time as compared to RISC.
10. T/F – Superscalar and superpipelining are methods that intend to maximize the number of instructions that can be executed.

Instruction to students: Answer questions 1-10 into this table

Question number	1	2	3	4	5	6	7	8	9	10
True										
False										

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Part 2 : Multiple Choice Questions: **(20 points)**

Instruction to students: Answer questions 11-30 into this table

Num	A	B	C	D		Num	A	B	C	D
11						21				
12						22				
13						23				
14						24				
15						25				
16						26				
17						27				
18						28				
19						29				
20						30				

11. Address of the next instruction can be obtained from
    A. Opcode B. Program counter
    C. Instruction queue D. Any of the above

12. Data transfer type instruction can involve
    A. Data to & from memory B. Data between registers
    C. Data between I/O D. All of the above

13. These operation may involve the DMA controller
    A. Arithmetic instructions B. I/O Instructions
    C. Logical instructions D. None of the above

14. Branches and jumps are types of
    A. Arithmetic instructions B. Data or Logical instructions
    C. I/O instructions D. Transfer of control instructions

15. The type of addressing mode and operand information is obtained in which part of the instruction cycle?
    A. Fetch B. Issue
    C. Execute D. Decode

16. The CPU system bus involves transfer of
    A. Control B. Data
    C. All of the above D. Instruction

17. These registers are set during the execution of an instruction
    A. Data registers B. Address Registers
    C. Control D. Condition code

18. In pipelining there is a requirement of this between stages
    A. Memory B. Registers
    C. Buffer D. None of the above

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19. This type of instruction does not need a write back stage
    A. Load B. Store
    C. Add D. Multiply

20. If a source operand of an instruction is the destination of the previous instruction, it leads to a
    A. Control hazard B. Register hazard
    C. Structural hazard D. Data hazard

21. The a vital characteristic of a procedure call is
    A. When it is called B. Called by whom
    C. Amount of nesting D. All of the above

22. Storage space that has the fastest access time
    A. Cache B. Main Memory
    C. Hard drive D. Registers

23. The instruction set of a CISC architecture is
    A. Very simple B. Highly complex
    C. Similar to RISC D. None of the above

24. The number of instruction types available in the CISC architecture makes the program,
    A. Smaller B. Longer
    C. Does not change D. None of the above

25. Compared the CISC, RISC architecture has
    A. Simpler opcode B. Simple addressing modes
    C. Fewer load/store D. All of the above

26. Example of techniques that increase pipeline efficiency
    A. Delayed load B. Delayed branch
    C. Loop unrolling D. All the above

27. Parallelism is increased by using this pipeline technique
    A. Superscalar B. Simplescalar
    C. Multiple Execution steps D. None of the above

28. Type of data dependency
    A. RAW B. WAR
    C. WAW D. All of the above

29. Degree of instruction parallelism depends on
    A. Data dependency B. Procedural dependency
    C. Frequency of A D. Frequency of A&B

30. A LOAD instruction is said to be complete when the data is read and written onto?
    A. Memory-Memory B. Memory-Register
    C. Memory-ALU D. None of the above

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Part 3: Fill in the blanks **(20 points)**

31. Instruction are represented as _____ bits and is called _____.

32. The _____ stores the most significant bit in the highest numerical address.

33. The type of data transfer is dependent upon the addressing _____ used in the instruction.

34. A procedure call within a procedure call is called _____.

35. A collection of different types of instructions with various addressing modes is called _____.

36. The number of address bits determines the _____ that can be referenced.

37. _____ is the a software program used to convert a high level program in assembly language.

38. The _____ is used convert assembly language into machine language that can be executed by the hardware. .

39. _____ involves breaking up of the instruction cycle to speed up the execution.

40. Pipelining in general calls for an increase in the number of _____ used.

41. If two consecutive instructions require the one single arithmetic unit, it leads to a _____ hazard.

42. When operand references are highly localized, the property of instructions is termed as _____ locality.

43. Adding a _____ memory can speed up the performance of a Random Access memory

44. An important characteristic of a RISC machine is that all transfers within instructions must be _____ to _____ .

45. RISC architecture inherently tries to prevent extensive use of _____ instructions.

46. The R4000 is a _____ processor.

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47. A _____ is used to stall the pipeline.

48. In Super-pipelining approach, the number of cycles required to execute a single pipeline stage is _____.

49. _____ limits execution of two instructions requiring the same arithmetic unit in _____.

50. Resource conflicts in a pipeline can be reduced by _____resources.

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Part5 : Processor Design and Parallel architecture

51. Design the datapath of a 32 bits CPU with the following specifications

- 8 general purpose registers (R0-R7), all registers are 32-bit wide
- Fixed-length (32 bits) instructions
- 1 Stack Pointer
- 16-bit external databus
- Instructions and data are stored in the memory using little endian style
- Cache memory and cache controller are not included in the CPU

51.1 Draw the datapath of the CPU (5 points)

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51.2 Write the register transfer notation of the fetch operation and the corresponding active control signals of each step (2.5 points)

	Micro-Operations	Active control signals
Fetch cycle	.....	.....
	.....	.....
	.....	.....
	.....	.....
	.....	.....
	.....	.....
	.....	.....
	.....	.....
	.....	.....
	.....	.....

51.3 Write the register transfer notation of the execution phase of instruction **PUSH Rn** (2.5 points)

	Micro-Operations	Active control signals
Execute cycle Of **PUSH Rn**	.....	.....
	.....	.....
	.....	.....
	.....	.....
	.....	.....
	.....	.....
	.....	.....
	.....	.....
	.....	.....
	.....	.....

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52. The CPU shown in figure 1 is used for questions 52 and 54. Assume that the instruction cycle of this CPU contains only 2 phases: fetch and execution.

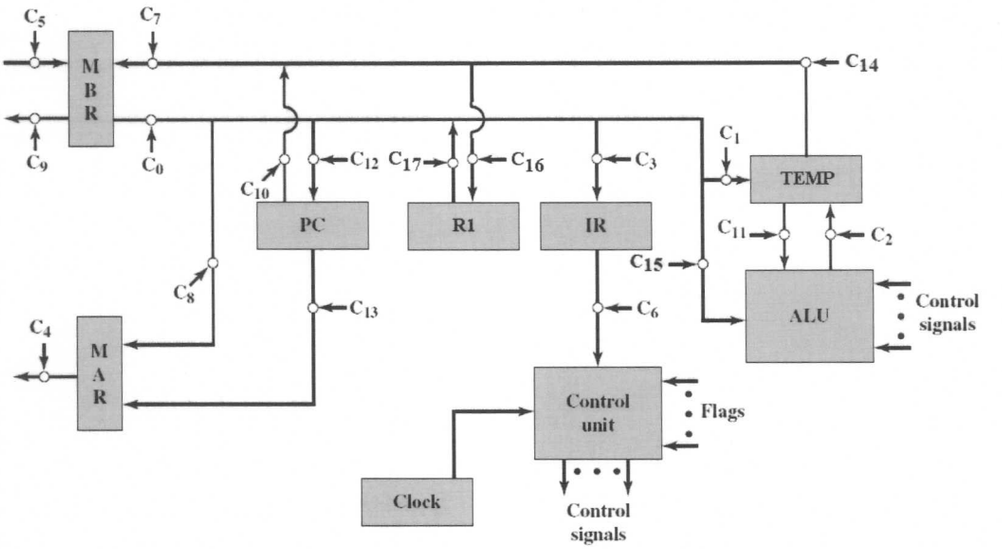

Figure 1- datapath of the CPU

Table 1 – Register transfer notation of the fetching operation and the execution phase of 2 instructions.

Fetch phase	Execution phase of INC **x**	Execution phase of ADD R1, **x**
t1: MAR ← (PC) t2: MBR ← Memory PC ← (PC) + I t3: IR ← (MBR)	t1: MAR ← IR(address) t2: MBR ← Memory t3: TEMP←(MBR)+1 t4: MBR ← (TEMP) t5:Memory←(MBR)	t1: MAR ← IR(address) t2: MBR ← Memory t3: TEMP ← (R1) t4: TEMP←(MBR)+(TEMP) t5: R1 ← (TEMP)
Note: **x** is the memory location		

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Suppose that the hardwired control unit of this CPU is made from the block diagram shown in figure 2.

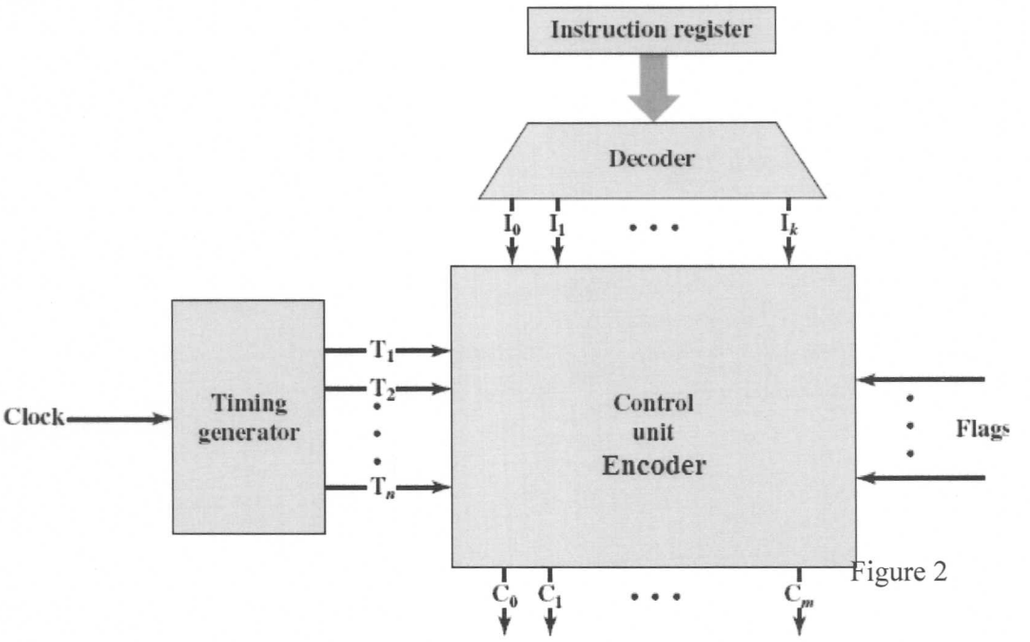

Figure 2

52.1 Design the circuit of the hardwired control unit encoder for creating the C_5 signal (3 points)

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52.2 Design the circuit of the hardwired control unit encoder for creating the C_3 and C_8 signals (3.5 points)

52.3 Design the circuit of the hardwired control unit encoder for creating the C_2 and C_{14} signals (3.5 points)

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53. Suppose the program A takes 60 minutes running on 1 CPU system. Calculate the time requiring for running the modified version of this program on a 100-CPUs system. Suppose that 60 % of the tasks this program can be fully parallelized. (5 points)

54. Design the micro-programmed control unit for the CPU in figure 1. Assume that the block diagram of this control unit is shown in figure 3.

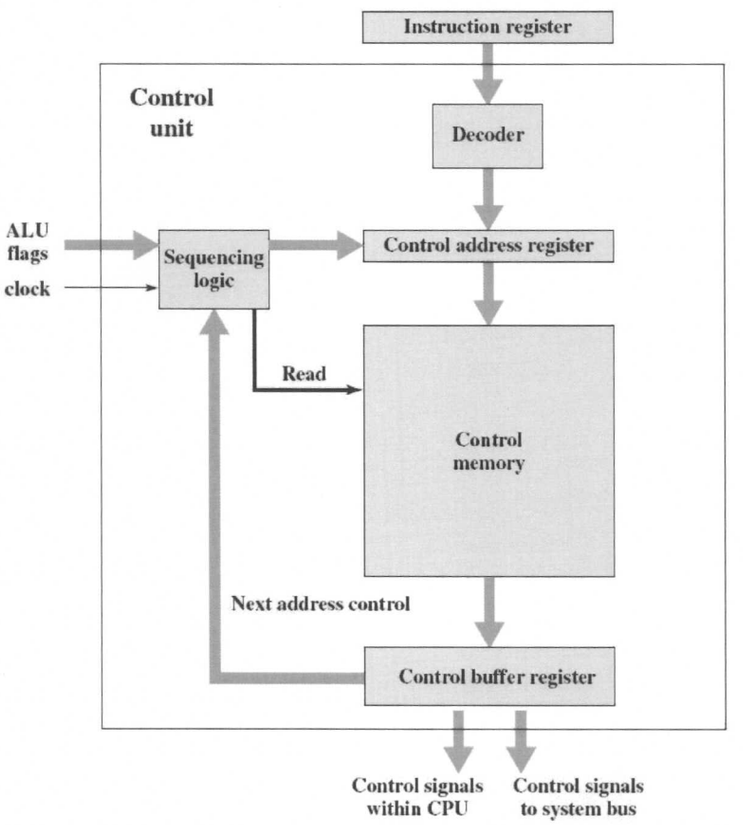

Figure 3

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Fill all the blank fields of the data in the control memory (10 points) (**suggestion:** see figure 1 and table 1 on page 9)

Control store address	Next address (binary value)					Control Signals (Active high)																		Routine type
	A4	A3	A2	A1	A0	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16	C17	
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	Fetch Routine
1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
2	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
3																								INC X routine
4																								
5																								
6																								
7																								
8																								Add R1,X routine
9																								
10																								
11																								
12																								

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55. Consider the program shown in figure 4 and answer questions 55.1-55.3

```
shared integer array a[1..N], b[1..N]
shared integer dot_product
shared lock dot_product_lock
shared barrier done
.
.
read a[1..N] from vector_a
read b[1..N] from vector_b
dot_product := 0
create_thread (do_dot, a, b)
do_dot (a,b)
print dot_product
.
.
do_dot (integer array x[1..N], integer array y[1..N])
      private integer local_dot_product
      private integer id
      id :=mypid()
      local_dot_product := 0
      for k:=(id*N/2)+1 to (id+1)*N/2
            local_dot_product := local_dot_product + x[k] * y[k]
      end
      lock (dot_product_lock)
            dot_product := dot_product + local_dot_product
      unlock (dot_product_lock)
      barrier (done)
end do_dot
```

Figure 4 – Parallel program for computing dot product.

55.1 How many CPUs does the program shown in figure 4 support? (1 points)

.....

55.2 What kind of architecture (using Flynn's taxonomy) suitable for running this program? (1 points)

.....

55.3 Explain how to modify the program shown in figure 4 to support ***n*** CPUS, where ***n*** is the number of the available processing elements in the system. (3 points)

.....
.....
.....
.....
.....
.....
.....
.....
.....
.....

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56. A multiprocessor system contains 5 single-core Pentium4 CPUs. The cache coherency of these CPUs is the MESI protocol, as shown in figure 5. Use this diagram to answer questions 56.1 and 56.2

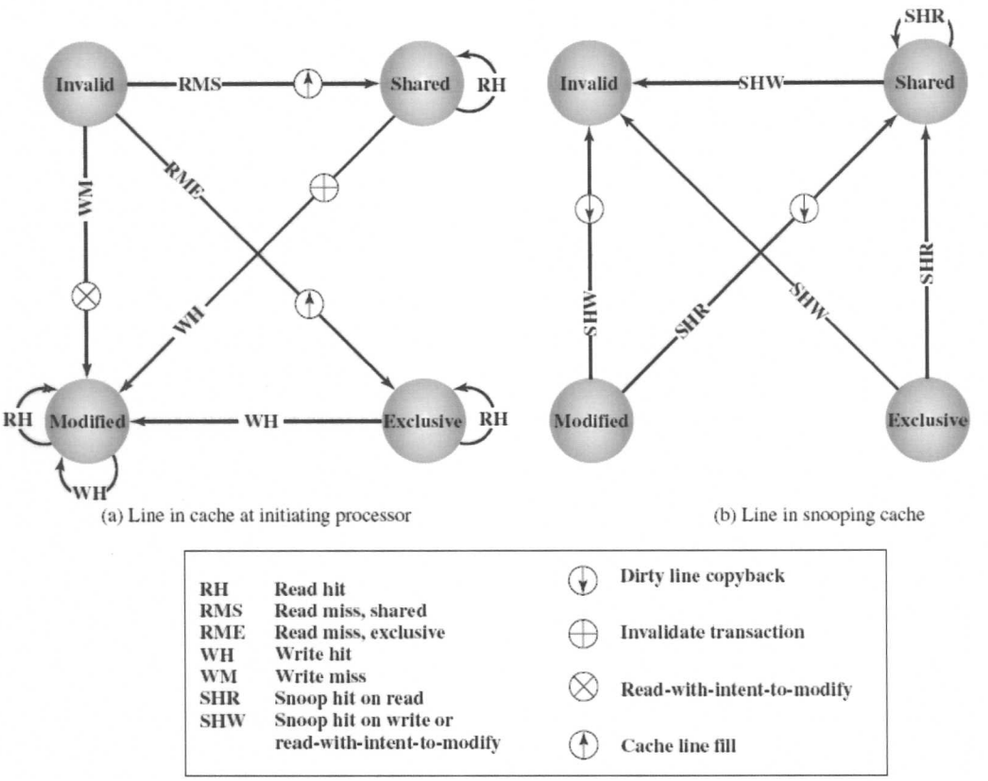

Figure 5: MESI protocol

The sequence of events on this 5-CPUs system occurs like this…

time	11.00:00am	CPU1 executes instruction MOV AX, [0x100]
time	11.12:10am	CPU1 executes instruction MOV AX, 0x50
time	11.12:20am	CPU1 executes instruction MOV [0x100], AL
time	11.12:30am	CPU3 executes instruction MOV AL, [0x100]
time	11.12:40am	CPU4 executes instruction MOV AH, [0x100]
time	11.12:50am	CPU1 executes instruction INC [0x100]
time	11.12:60am	CPU2 executes instruction MOV [0x100], AH
time	11.12:70am	CPU4 executes instruction DEC [0x100]
time	11.12:80am	CPU2 executes instruction MOV [0x100], AL

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56.1 Fill the status of AX register and cache line of CPU1 for each specific time into the following table (5 points)

Time	Data in the cache line for keeping value from mem[0x100]	Cache status of the line keeping mem[0x100]	Previous status of Cache Operation	Data in AH	Data in AL
11.12:05	0x60	Exclusive	Read miss	0x30	0x60
11.12:15	0x60	Exclusive	No cache access	0x00	0x50
11.12:25					
11.12:35					
11.12:45					
11.12:55					
11.12:55					

56.1 Fill the status of AX register and cache line of CPU2 for each specific time into the following table (5 points)

Time	Data in the cache line for keeping value from mem[0x100]	Cache status of the line keeping mem[0x100]	Previous status of Cache Operation	Data in AH	Data in AL
11.12:55	No value from mem[0x100] in the cache	-	-	0x77	0x44
11.12:65					
11.12:75					
11.12:85					

------- *End of Examination* -------