



มหาวิทยาลัยสงขลานครินทร์
คณะวิศวกรรมศาสตร์

สอบกลางภาค: 2nd Semester

ปีการศึกษา: 2554

วันที่สอบ: December 19, 2011

เวลาสอบ: 13.30 – 16.30

ห้องสอบ: A401

ผู้สอน: Dr.Taweesak

รหัสวิชาและชื่อวิชา: 241-535 Testing and Testable Design of Digital Systems

Allowed Materials: Text books and calculator

Disallowed Material: Laptop

Exam Duration: 3 Hours (180 Minutes)

Suggestions

- Exam is contained 6 pages (including cover page) 5 problems; total scores 35 %.
- If any part of answers is illegible, it will be judged to be wrong.
- Read questions carefully.
- Allowed to write on both sides of the answer sheet.

Name _____ Student I.D. _____

1) In the figure 1, find solution(s) of each question.

(7 marks)

1.1) Calculate number of single faults.

1.2) Calculate number of collapsed faults.

1.3) Write a truth table in order to compare fault-free circuit and faulty circuit by using Stuck-at fault model and also identify all detected faults.

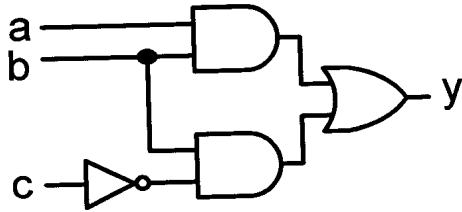


Figure 1

2) In the figure 2, find solution(s) of each question.

(8 marks)

- 2.1) Identify all problems for testing the circuit without using scan design.
- 2.2) Modify the circuit by replacing all flip-flops with the muxed-D scan cells.
- 2.3) Describe how the circuit in 2.2) can fix the problems in 2.1).
- 2.4) Explain the sequence of test operation related to clock signal (CLK). Assume that test data of muxed-D scan cells is 110 and the data of test response is 010.

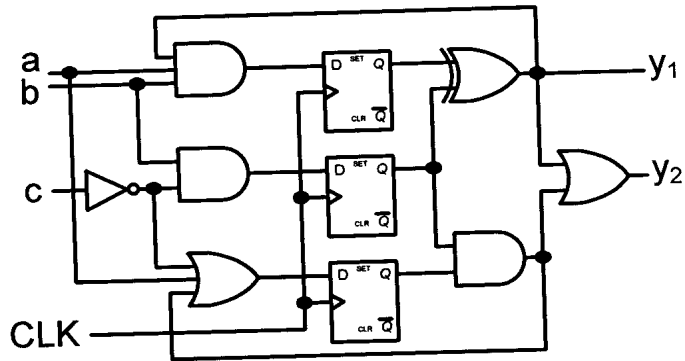


Figure 2

3) There are 3 types of the scan architecture: Full-scan Design, Partial-scan Design and Random-access Scan Design. Find solution(s) in the following questions. (6 marks)

3.1) Compare advantages and disadvantages of 3 types of scan architecture into a table.

3.2) Identify the suitable situations (or conditions). in order to apply the partial-scan design for testing.

4) In figure 4, show the timing diagram related to timing model in the following conditions:
(6 marks)

- 4.1) Nominal Delay: 2-input gate 1 ns; 3-input gate 1.2 ns; inverter 0.6 ns
Inertial Delay: all gates 0.3 ns
- 4.2) Rise Delay: 2-input gate 0.8 ns; 3-input gate 1 ns; inverter 0.6 ns
Fall Delay: 2-input gate 1 ns; 3-input gate 1.2 ns; inverter 0.8 ns
- 4.3) Minimum Delay: 2-input gate 0.8 ns; 3-input gate 1 ns; inverter 0.6 ns
Maximum Delay: 2-input gate 1 ns; 3-input gate 1.2 ns; inverter 0.8 ns

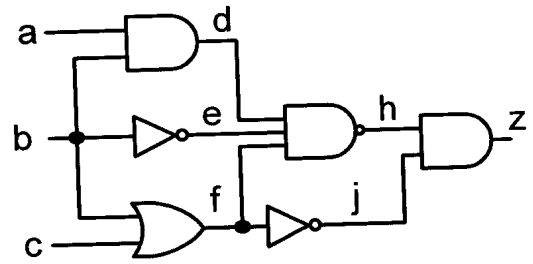
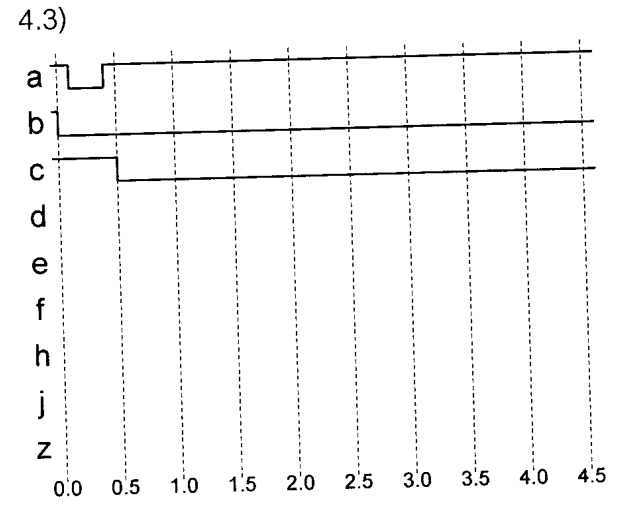
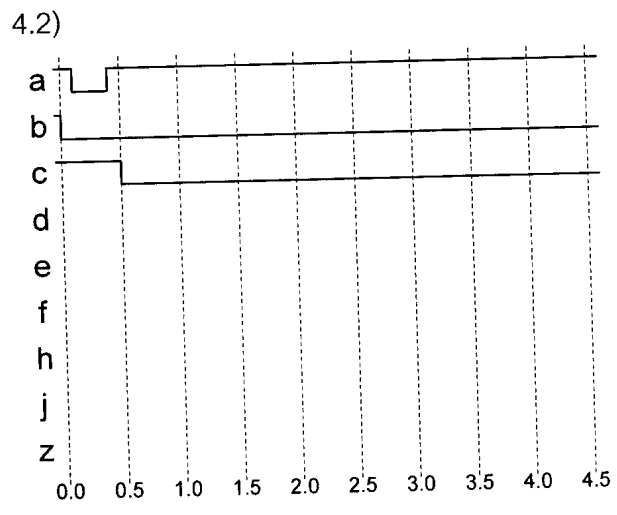
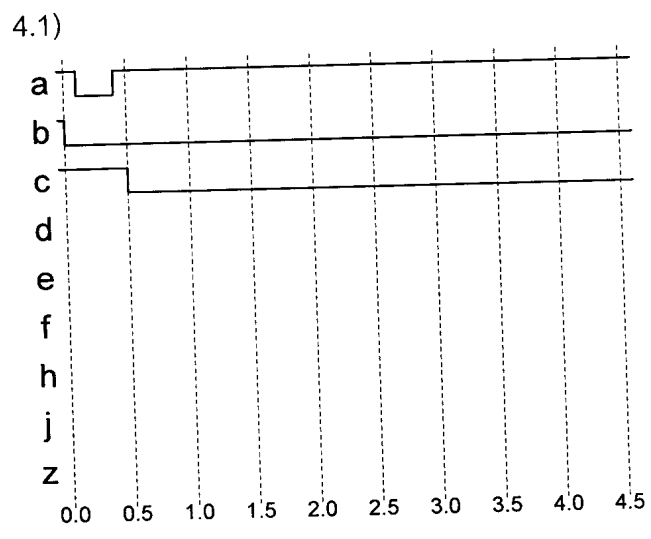


Figure 4



5) In figure 5, show the fault list at the output y based on deductive fault simulation. Assume test patterns are $abc = 001, 100,$ and 010 respectively. (8 marks)

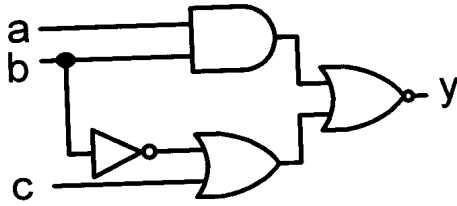


Figure 5