

Name ..... Student ID .....

## มหาวิทยาลัยสงขลานครินทร์

## คณะวิศวกรรมศาสตร์




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สอบกลางภาค: ภาคการศึกษาที่ 2	ปีการศึกษา: 2557
วันที่สอบ: 18 มีนาคม 2558	เวลาสอบ: 13.30-15.30น.
รหัสวิชา: 242-461	ห้องสอบ: A200
ชื่อวิชา: Broadband Integrated Networks	อาจารย์ผู้สอน: อ.สินชัย กมลภวิงศ์

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อ่านรายละเอียดของข้อสอบ และคำสั่งให้เข้าใจก่อนเริ่มทำข้อสอบ

ไม่อนุญาต : - หนังสือและสมุดโน้ต  
- เครื่องคิดเลข

อนุญาต : - เครื่องเขียนต่างๆ เช่น ปากกา หรือดินสอ

เวลา : 2 ชั่วโมง (120 นาที)

รายละเอียดของข้อสอบ : ข้อสอบมีทั้งหมด 14 หน้า (รวมปก)

คำสั่ง :

- คำตอบทั้งหมดจะต้องเขียนลงในสมุดคำตอบ
- เขียนคำตอบลงในเอกสารนี้เท่านั้น
- คำตอบส่วนใดอ่านไม่ออก จะไม่ตรวจคำตอบนั้น

-- ทูจริติในการสอบมีโทษขั้นต่ำปรับตกในรายวิชานี้ และพักการเรียน 2 ภาคการศึกษา --

-- โทษสูงสุดคือ ไล่ออก --

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**1. Switching Architecture**

1.1 What are the main differences between “Space Switching”, “time Switching” and “Statistical Switching” (5 marks)

Answer

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1.2 What are the differences between open loop and closed loop flow control? (5 marks)

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1.3 What are the differences between preventive flow control and reactive flow control? (5 marks)

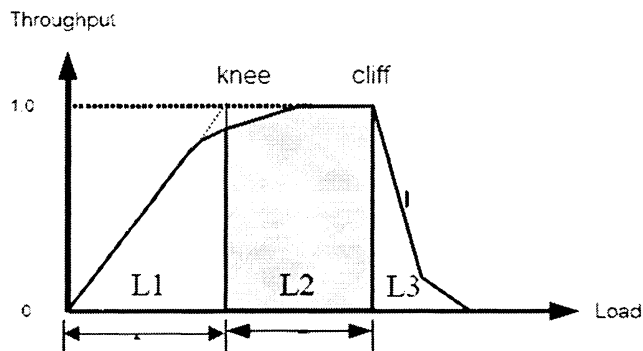


Figure 1 Load and Throughput

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1.4 From the given **Error! Reference source not found.** below, please explain how each step works (HUNT Mode, PRESYNC Mode and SYNCH Mode) (10 marks)

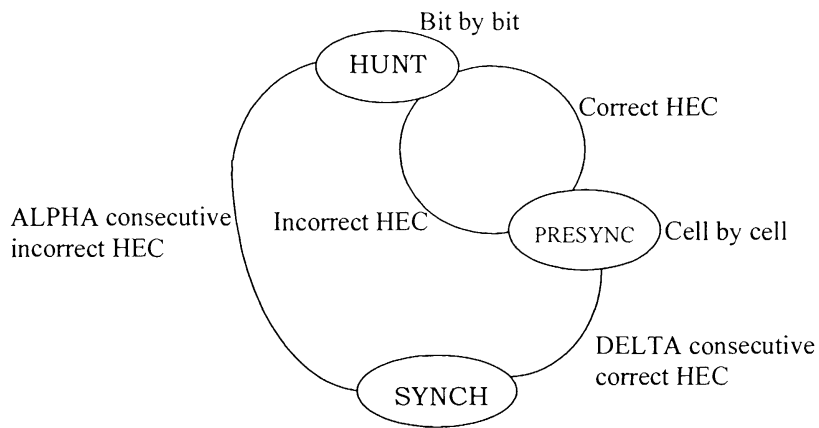


Figure 2 for question no. 2

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2. 3-stage delta network

Cell A and cell B enter to ATM switch as shown in the below picture. ATM switch architecture is a 3 Stages of Delta Network. Routing table is ATM switch is assigned below

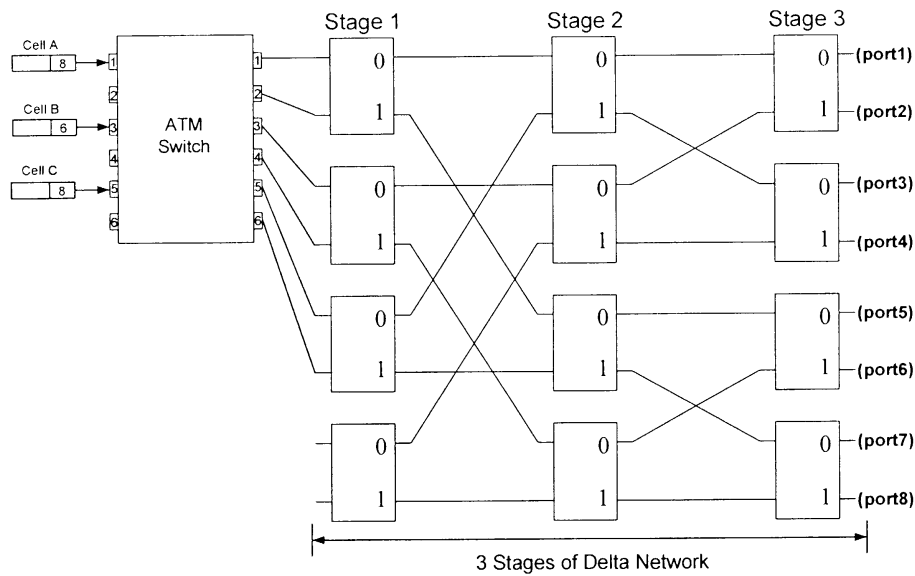


Figure 3 3-stage Delta Network Switch

Port In	VCI In	VCI Out	Port Out	Internal Header
1	6	10	1	0,1,1
1	8	15	2	1,1,1
3	6	18	3	1,0,1
3	8	20	4	0,1,0
5	6	22	5	0,0,1
5	8	18	6	1,0,0

Table 1 Cell routing table in ATM Switch

3.1 What are the output ports of cell A, B and C? (5 marks)

**Answer:**

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3.2 If we want cell A routed to output port number 7, what the internal header values for cell A are (5 marks).

**Answer:**

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3. Below is the 8 x 8 Knockout Switching Element structure (Input 8 ports, Output 8 ports) with 8 x 4-type concentrators (Input 8 ports, Output 4 ports). Answer the following questions.

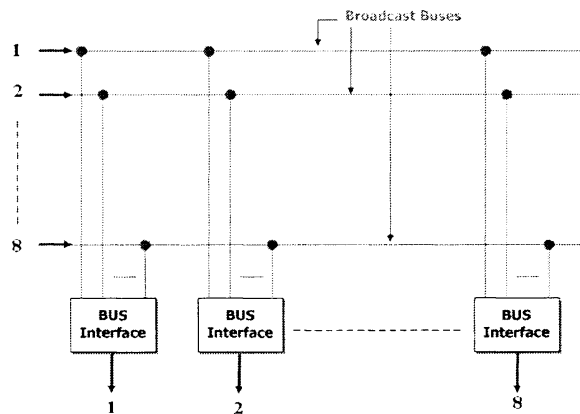


Figure 4: Knockout Switching Element

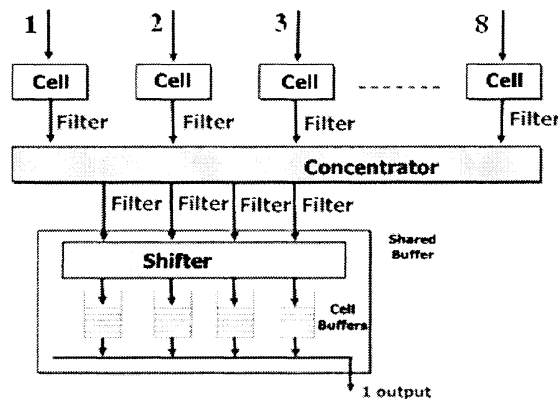


Figure 5 Output unit of Knockout Switch

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4.1 How many rows of cell buffers are required in this Knockout Switching Element structure? (5 marks)

**Answer:**

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4.2 If there are 8 cells of data and each cell of the 8 cells enters each input port simultaneously with all the 8 cells exiting at one same output port number 1, how many cells are dropped? (5 marks)

**Answer:**

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4. Explain how EFCI (Explicit Forward Congestion Indication) works, please draw a graph of the source node behavior in terms of traffic load (X axis is time, Y axis is source load).(10 points)

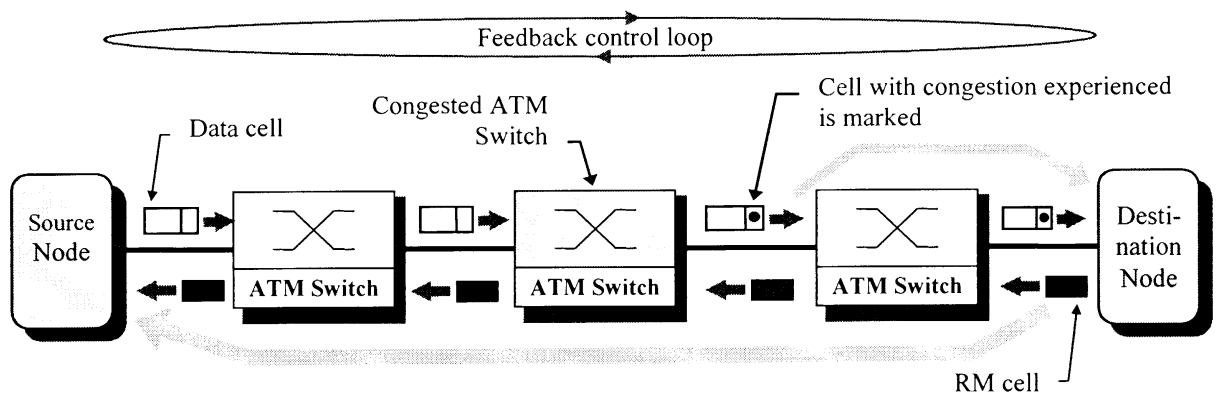


Figure 6 EFCI flow control

**Answer**

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6. **Error! Reference source not found.** shows VBR traffic time slots (in cell time). Please show that which VCR cells are conform and non-conform using Generic Cell Rate Algorithm (GCRA) parameters as follows: (15 marks)

$T(\text{PCR}) = 1$  cell time,  $\tau(\text{PCR}) = 0$  cell time  
 $T(\text{SCR}) = 4$  cell time,  $\tau(\text{SCR}) = 3$  cell time  
 $MBS = 3$  cells

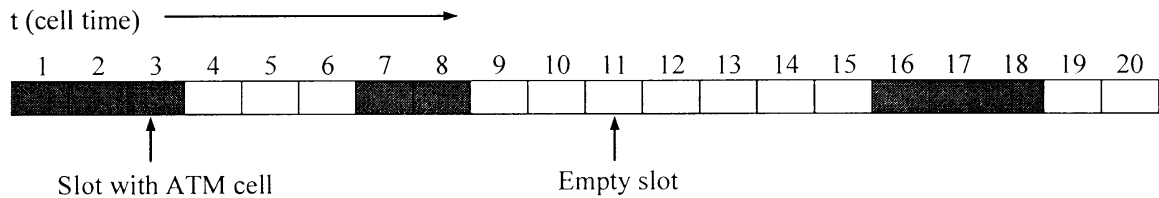


Figure 7 VCR traffic arrival time

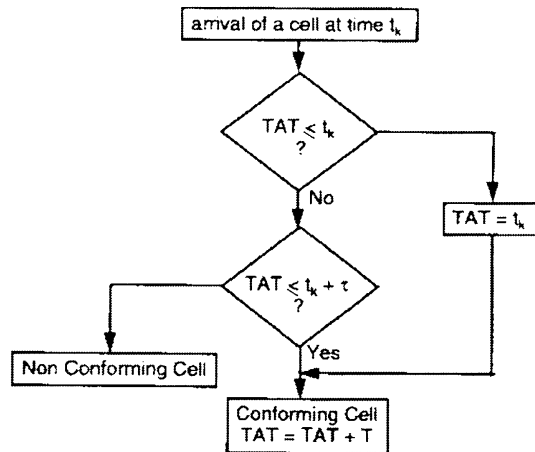


Figure 8 Generic Cell Rate Algorithm

**Answer:**

GCRA1 evaluation

$T(\text{PCR}) = \underline{\hspace{1cm}}$  cell time,  $\tau(\text{PCR}) = \underline{\hspace{1cm}}$  cell time

t = 1: TAT = 1, conforming, TAT = 1 + 1 = 2

t = 2: TAT = .....

t = 3: TAT = .....

t = 7: TAT = .....

t = 8: TAT = .....

t = 16: TAT = .....



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t = 17: TAT = .....

t = 18: TAT = .....

GCRA2 evaluation:

T(PCR) = \_\_\_ cell time,  $\tau$ (PCR) = \_\_\_ cell time

t = 1: TAT = 1, conforming, TAT = 1 + 4 = 5

t = 2: TAT = 5, t +  $\tau$  = 5, conforming, TAT = 5 + 4 = 9

t = 3: TAT = .....

t = 7: TAT = .....

t = 8: TAT = .....

t = 16: TAT = .....

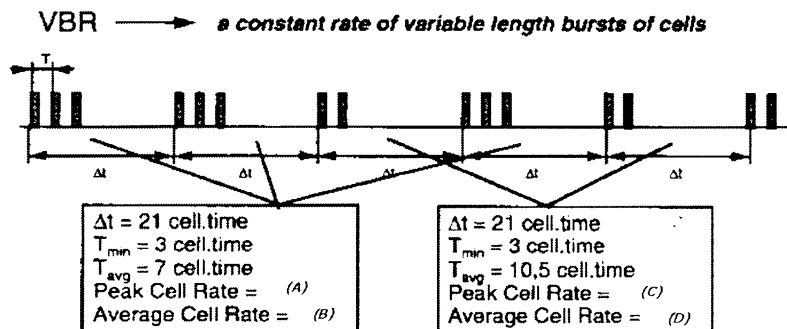
t = 17: TAT = .....

t = 18: TAT = .....

7. Below is the calculation of CAC (call admission control) for VBR Traffic, please give the values of MBS, and Required buffer (5 marks)

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|---|--|
| 1. Assume that all connections are compliant with GCRA(1/PCR <sub>i</sub> , 0) and GCRA(1/SCR <sub>i</sub> , $\tau_s$ ).    | 1. GCRA(1,0) and GCRA(3,8)                           |
| 2. Determine N, the maximum number of sources $N \times SCR_i \leq PCR_o$ .   | 2. PCR <sub>o</sub> = 1, SCR <sub>i</sub> = 1/3, N=3 |
| 3. Find out the worst case for one source with MBS = integer{(1 + ( $\tau_s$ /(1/SCR <sub>i</sub> - 1/PCR <sub>i</sub> )))} | 3. MBS = <input type="text"/>                        |
| 4. Assume that all sources are synchronised and transmit their worst case traffic.  | 4. <input type="text"/>                              |
| 5. Find the buffer size to avoid any overflow Req_Buf = (N - PCR <sub>o</sub> /PCR <sub>i</sub> ) x MBS                     | 5. Req_Buf = <input type="text"/>                    |
| 6. Compute the maximum delay $D \leq Req\_Buf / PCR_o$  | 6. D ≤ 10 cells                                      |

Please fill in the number taken from the traffic condition below: (10 marks)



(A) = .....

(B) = .....

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(C) = .....

(D) = .....

**- Gigabit Ethernet.**

9. In Gigabit Ethernet, It operates on 2 modes: shared access, and dedicated-access. Gigabit Ethernet uses CSMA/CD for shared-access with 2 important modifications. What are they? (10 marks)

Answer

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10. Gigabit Ethernet has dedicated-access topology enhancement. This mode is used for point-to-point connection and operated in full-duplex. In the full-duplex mode, CSMA/CD is disabled, and introducing link-level flow control. Please draw a ***“flow chart”*** how link-level flow control works (10 marks).

Answer

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11. Gigabit Ethernet at PCS uses 8B/10B encoding. Next, the PMA sublayer is the part of GMII responsible for providing a medium independent for the PCS to support serial bit-oriented physical media. To do this, the PMA serializes code groups for transmission and de-serializes bits received from the medium into code groups. For fiber operations the PMD sublayer becomes responsible for mapping the physical medium to the PCS. Note that the MDI represents the physical layer interface and is part of the PMD. If the information (as shown below) inputs to the 8B/10B encoder. What is the information value after encoding? (5 marks). Why do we need this encoder? (5 marks)

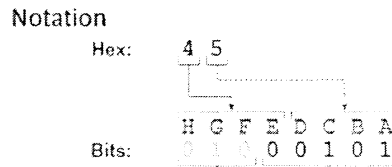


Figure 9 Data format

Answer

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12. From figure below, please explain how this multiplex works, to form one lane to  $n$  lane. This is 40 GbE. The input is from 64/66b words. (10 marks)

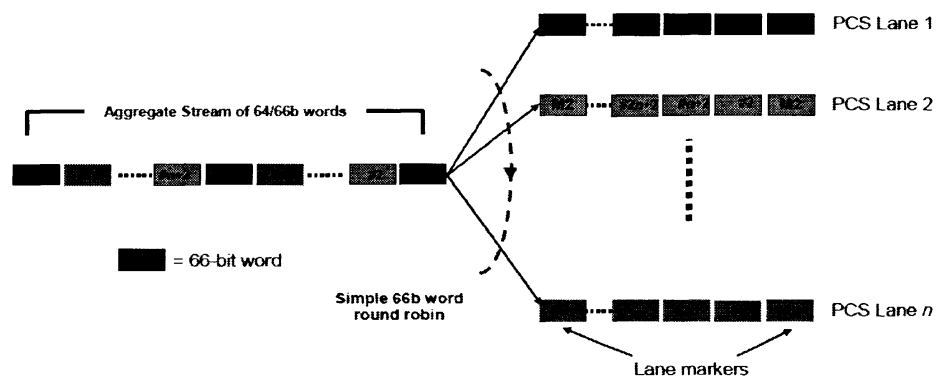


Figure 10 PCS Lane Distribution Concept

Answer

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