Student Name ..... ID: .....

มหาวิทยาลัยสงขลานครินทร์

คณะวิศวกรรมศาสตร์

สอบกลางภาค: ภาคการศึกษาที่ 2 **ปีการศึกษา**: 2558

วันที่สอบ: 2 มีนาคม 2559 **เวลาสอบ**: 13.30-15.30น.(2 ชั่วโมง)

รหัสวิชา: 242-461 **ห้องสอบ**: A200

ชื่อวิชา: Broadband and High Speed Networks **อาจารย์ผู้สอน:** อ.สินชัย กมลภิวงศ์

อ่านรายละเอียดของข้อสอบ และคำสั่งให้เข้าใจก่อนเริ่มทำข้อสอบ

ไม่อนุญาต : - หนังสือและสมุดโน้ต

- เครื่องคิดเลข เครื่องอิเล็กทรอนิกส์ทุกชนิด

อนุญาต : - เครื่องเขียนต่างๆ เช่น ปากกา หรือดินสอ

เวลา : 2 ชั่วโมง (120 นาที)

รายละเอียดของข้อสอบ : ข้อสอบมีทั้งหมด _13_ หน้า (รวมปก)

คำสั่ง :

- ข้อสอบมีทั้งหมด _13_ หน้า ให้ทำทุกข้อ
- คำตอบทั้งหมดจะต้องเขียนลงในสมุดคำตอบ
- คำตอบส่วนใดอ่านไม่ออก จะไม่มีคะแนนให้

-- ทุจริตในการสอบมีโทษขั้นต่ำปรับตกในรายวิชานี้ และพักการเรียน 1 ภาคการศึกษา --

-- โทษสูงสุดคือ ไล่ออก --

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PART I

1.1 What are the main differences between "Space Switching" and "time Switching"? (4 marks)

Answer

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1.2 What are the differences between open loop and closed loop flow controls? (4 marks)

Answer

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1.3 What are the differences between preventive flow control and reactive flow controls? (4 marks)

Answer

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2. Switch architecture: (15 marks)

Below is the 8 x 8 Knockout Switching Element structure (Input 8 ports, Output 8 ports) with 8 x 4-type concentrators (Input 8 ports, Output 4 ports). Answer the following questions.

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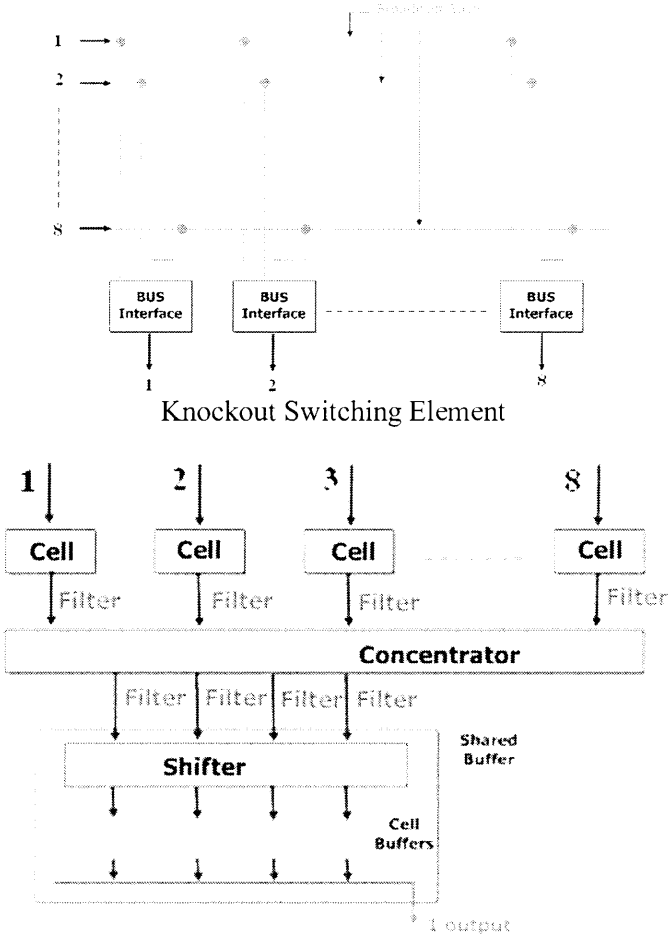

Figure 1 Use the above diagram in answering question no. 2.

2.1 How many rows of cell buffers are required in this Knockout Switching Element structure? (5 marks)

Answer

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2.2 If there are 8 cells of data and each cell of the 8 cells enters each input port simultaneously with all the 8 cells exiting at the same output port number 1, how many cells are dropped? (5 marks)

Answer

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3. Use the information in the table given below to answer the following questions:

ชนิดของสวิทช์แยกตามตำแหน่ง ของหน่วยเก็บข้อมูล		ขนาดหน่วยเก็บข้อมูล (เซลล์)	จำนวนสวิทช์ x ความเร็ว การสวิทช์	การทำงานของหน่วย เก็บข้อมูล	ข้อดี ข้อเสีย
เก็บข้อมูลที่เอาท์ พุท (output buffer)		100N	0(N) x NV	FIFO	-ควบคุมง่าย -เกิดการชนกันของ ข้อมูลที่บัสร่วม
เก็บข้อมูลที่ส่วน กลาง (central buffer)		100+10N	0(N) x NV	RIRO	-หน่วยเก็บข้อมูลมีขนาดเล็ก -การควบคุม หน่วยเก็บข้อมูลยุ่งยาก
เก็บข้อมูลที่อินพุท (input buffer)		< 100N	$0(N^2)$ x V	RIRO Contention	-ถ้าจะให้สมรรถนะสูง การควบคุมจะสลับซับซ้อน
สวิทช์ (crosspoint buffer)		100 (N^2)	$0(N^2)$ x V	FIFO Contention	- ควบคุมง่าย - หน่วยเก็บข้อมูลมีขนาดใหญ่

a. Which switch type does it use the largest memory? (5 marks)
b. Which switch type does it use the largest number of switching elements? (5 marks)
c. Which switch type does it use the fastest switching element? (5 marks)

Answer

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3. VBR Traffic and Performance Analysis
3.1 VBR Performance Analysis (10 marks)

Student Name ..... ID: .....

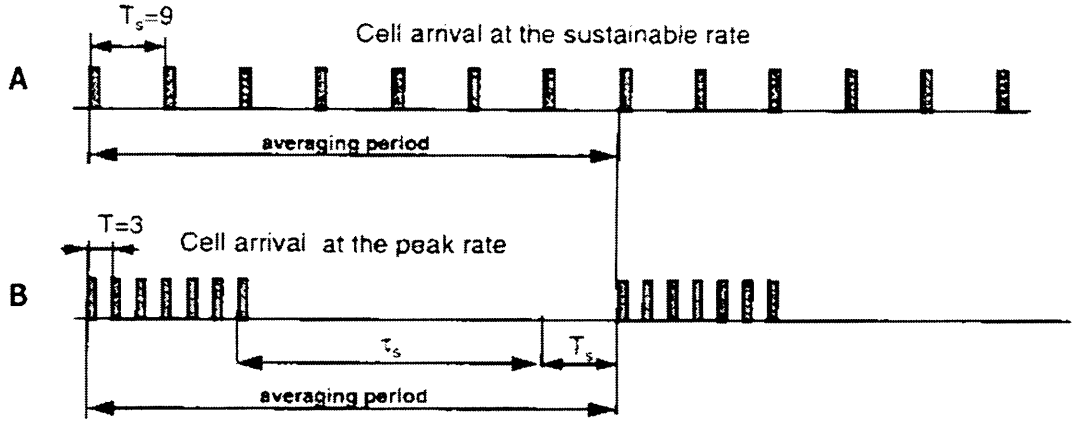

Figure 2 VBR Traffic Analysis

Figure 2 shows VBR traffic analysis as a sample scenario. Traffic A is CBR (Constant Bit Rate) Traffic where the peak and average cell rate is 9 cell.time. S is the size of the burst at peak rate. The assumption of VBR condition is a number of cell submitted during the period should be similar to CBR traffic condition. This means that Ts*S (Traffic A) is the same as Traffic B (VBR).
From the fiven Figure please find the maximum burst size (MBS) of this traffic condition.

Answer

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3.2 VBR Traffic (10 marks)

VBR traffic parameters submitted to ATM Network are:
PCR = 6000 cell/s SCR = 3000 cell/s MBS = 200 cell
While contact parameters between sources and switch are:
PCR = 360000 cell/s SCR = 3000 cell/s MBS = 1000 cell
What are the values of N (number of sources) can be admitted? (10 marks)

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Notation note:

- PCR: Peak Cell Rate specifies an upper bound on the traffic that can be submitted on the connection, T is the interval time between two consecutive cells where T=1/PCR,
- SCR: Sustainable Cell Rate (Rs) represents the upper bound on the realised average cell rate, where Ts is the average interarrival time.
- BT: Burst Tolerance is a number of the maximum cell at the peak cell rate which determine the Maximum Burst Size (MBS)
- CDV: Cell Delay Variation Tolerance represents the tolerance in relation to the Peak Cell Rate (PCR)

Answer

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4. The figure below, Figure 3, shows CBR traffic pattern in each time slot. By using GCRA (Generic Cell Rate Algorithm), shown in Figure 4, please show that which cells are non-conforming, and comforming. Please use the following parameters: T(PCR) = 5 cell time, τ(PCR) = 2 cell time (15 Marks).

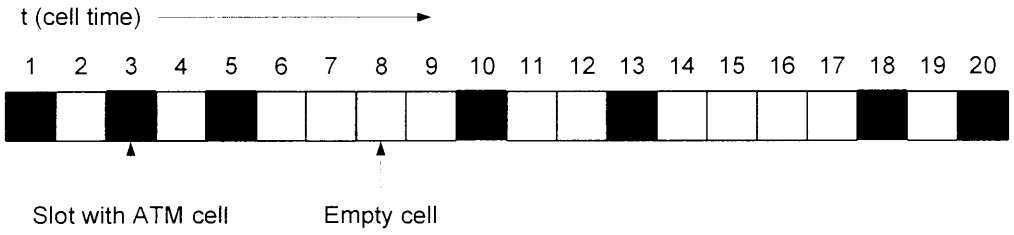

Figure 3 arrival of CBR traffic type in ATM time slots

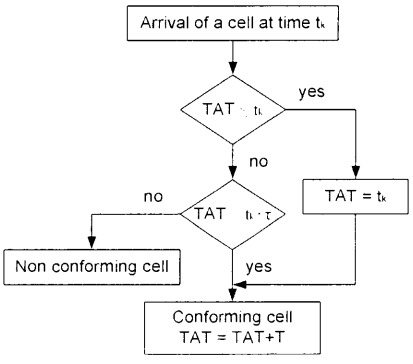

Figure 4 Generic Cell Rate Algorithms (GCRA)

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Answer

t = 1: TAT = 1, conforming, TAT = 1+5 = 6

t = 3: .....

t = 5: .....

t = 10: .....

t = 13: .....

t = 18: .....

t = 20: .....

5. The figure below, Figure 5, shows CBR traffic pattern in each time slot. By using GCRA (Generic Cell Rate Algorithm), shown in Figure 4, please show that which cells are non-conforming, and comforming. Please use the following parameters: (15 marks)

T(PCR) = 1 cell time, τ(PCR) = 0 cell time
T(SCR) = 3 cell time, τ(SCR) = 3 cell time
MBS = 3 cell

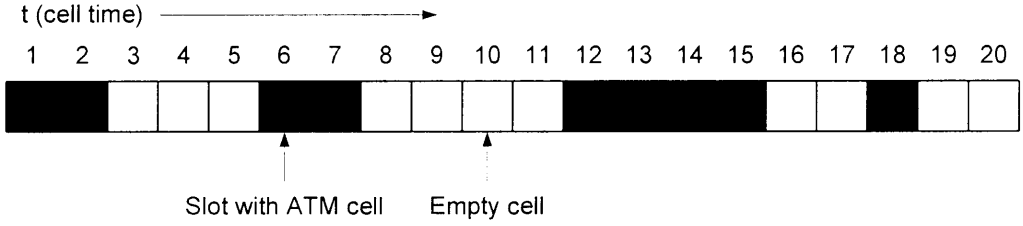

Figure 5 arrival of VBR traffic type in ATM time slots

Answer

t = 1: TAT = 1, conforming, TAT = 1+3 = 4

t = 2: .....

t = 6: .....

t = 7: .....

t = 12: .....

t = 13: .....

t = 14: .....

t = 15: .....

t = 18: .....

6. Below figure shows 'Head of line' blocking problem. Please give 2 solutions how to solve this problem (10 marks)

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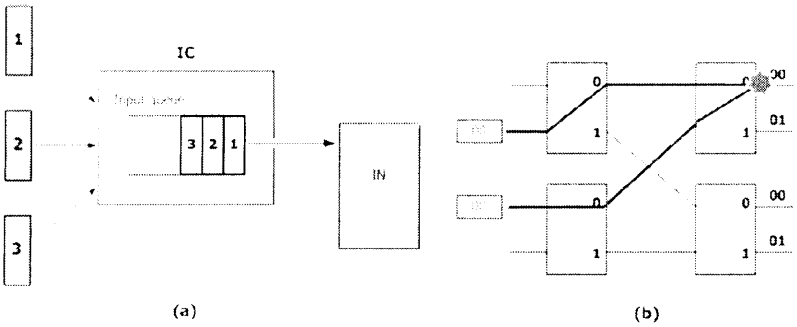

Figure 6 Head of Line blocking problem

Answer

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7. Below is a 8x4 concentrator switch. Please draw a routing line if input port is 2 and output port is 4 (10 marks)

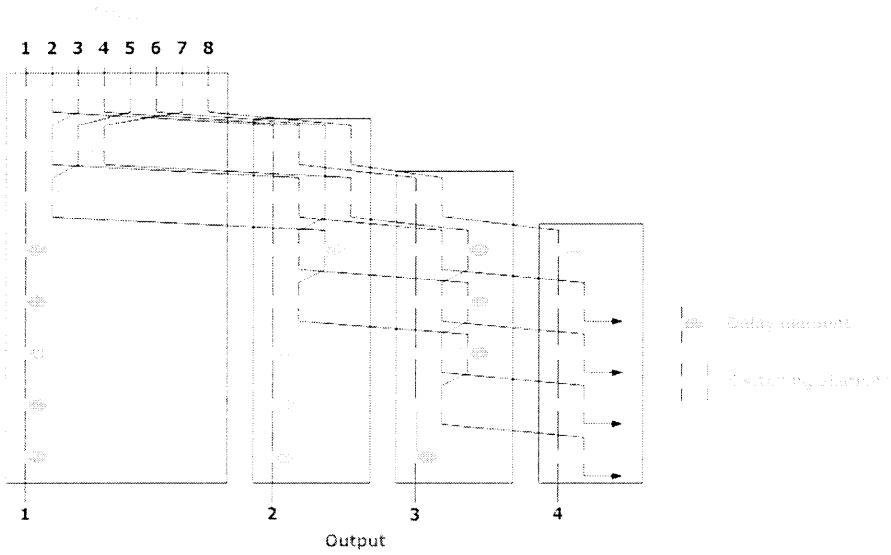

Figure - the *8x4 concentrator switch*

Answer

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8. Analog phone system
   8.1 Digital leased lines aim to deliver end-to-end data rate multiples of 64 Kbps up to 1,920 Kbps (in the case of Europe). How many voice channels can be accommodated?
   8.2 In North America, T1 digital LLs is a gross bit rate of 1.544 Mbps. How many voice channels can be accommodated? (10 marks)

Answer

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9. In xDSL, SHDSL and VDSL can offer symmetric operation. Please give at least 4 reasons why we need symmetric connection.
   Answer

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10. Below is how 'cross-talk' happens. Please give the type of each cross-talk indicated by A, B,C, and D (10 marks)

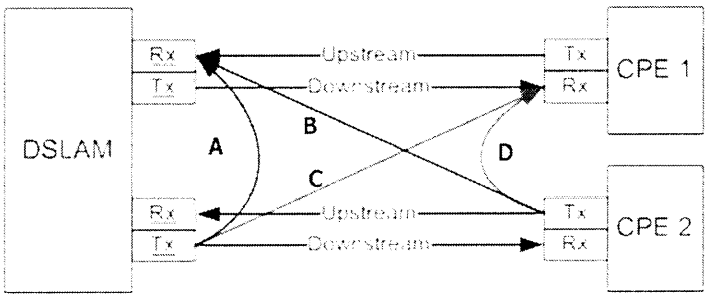

Figure x Cross-talk problems.

Answer

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11. Answer the following questions regarding to xDSL technology (10 marks)

13.1 Why does ADSL2+ achieve twice higher bandwidth than ADSL2?

13.2 Why VDSL2 can offer higher bandwidth than ADSL2?

Answer

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12. In Gigabit Ethernet, there are 2 important modifications, comparing to 10/100 Ethernet:

    a. Shared-access topology enhancement. Gigabit Ethernet uses CSMA/CD for shared-access with 2 important modifications. What are they? How they work (10 marks),

    b. Dedicated-access topology enhancement, how it works. What are the differences to CSMA/CD in terms of its mechanism (10 marks).

Answer

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13. Picture below shows how CSMA/CD works. Please insert the missing items (A) and (B).

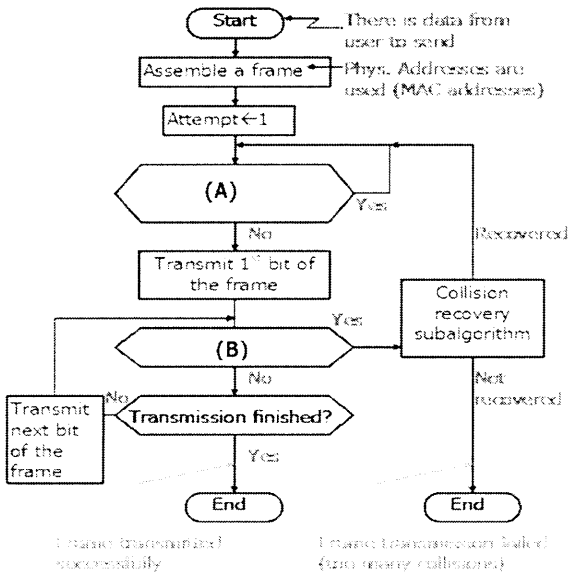

Figure 9 CSMA/CD protocol flow chart.

Answer

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14. Picture below demonstrates how 40G and 100G Ethernet work. The MLD scheme implemented in the PCS is fundamentally based on a striping of the 66-bit blocks across multiple lanes. Please explain how this scheme works. How many lanes are used for 40G and 100G Ethernet? (10 marks)

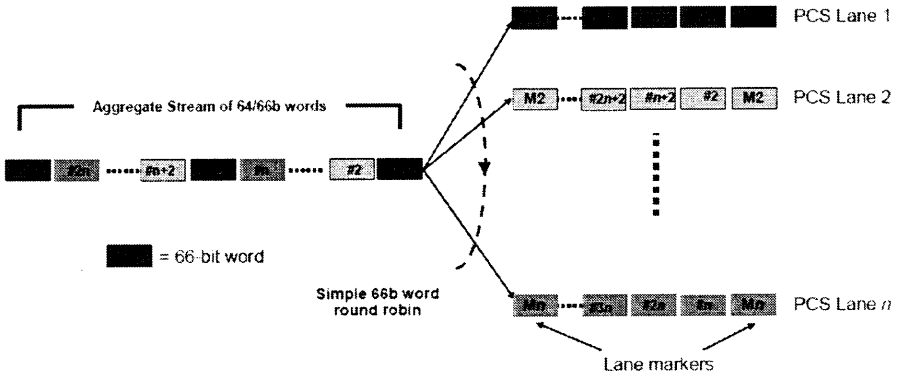

Figure 10 PCS Lane multiplexing in 40G and 100G Ethernet.

Answer

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15. Below is how 1Gbps can be achieved by Gigabit Ethernet, expanded from 100 Mbps Ethernet. Please show the calculation how 1 Gbps is obtained from twisted pair cable (10 marks)

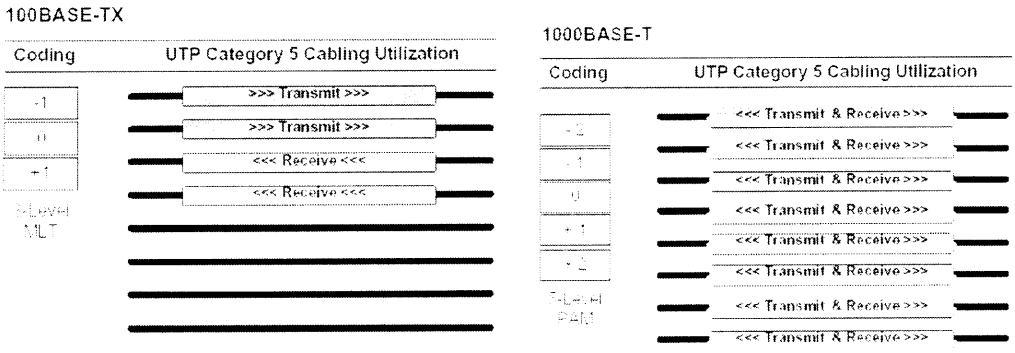

Figure 11 100Based-TX and 1000Based T line coding schemes.

Answer

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16. In 10/100 Mbps Ethernet, the smallest packet size is 64 bytes including all Ethernet overhead. According to Ethernet protocol limitation, please show how to calculate the maximum length of Ethernet segment, in case of using optical fiber link (10 marks) (Note, the average propagation delay in optical fiber is around 5usec per kilo-meter)

Answer

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